PCB Artist Quickstart Guide

Revision 01

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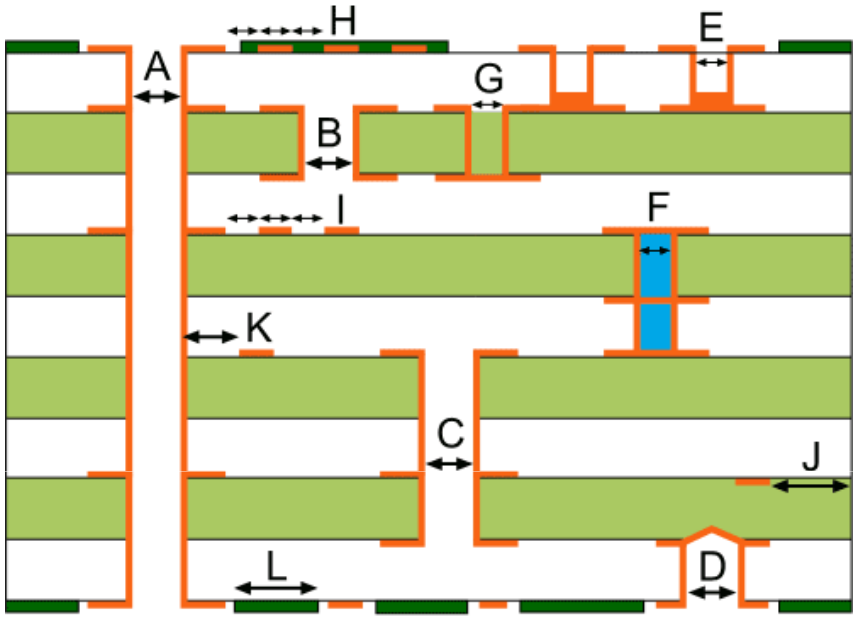
Analog Application Engineer-TI

Important Terminology

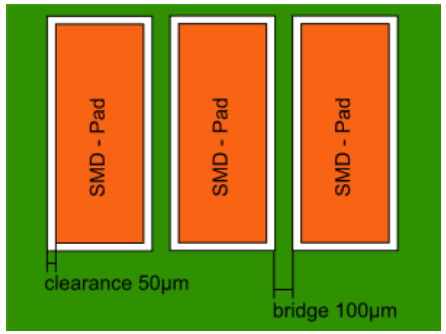
- PCB Artist is a free PCB schematic & layout tool provided by Advanced Circuits
- It can be downloaded from www.4pcb.com or www.download.com
- Pros:
  - Free
  - Intuitive and simple to use/install
  - Autorouter
  - Large libraries
  - East to create new parts (schematic symbols & footprints)
  - No minimum quantity for students (see website)
- Cons:
  - No interactive DRC
  - Boards are ~$33/ea (2-layer, 5 day turn) or $66/ea (4-layer, 5 day turn)
  - You do not get the gerber files (i.e. you must fabricate designs with Advanced Circuits)

Important Terminology

- "mil"
  - A "mil" is 1/1000th of an inch.
  - 1mil=.001"
- Layer
  - PCBs are made of 'layers'
  - Here are the common layers
    - Metal
      - The actual wires/conductors
    - Silkscreen
      - The white writing on the PCB
    - Soldermask
      - The green stuff



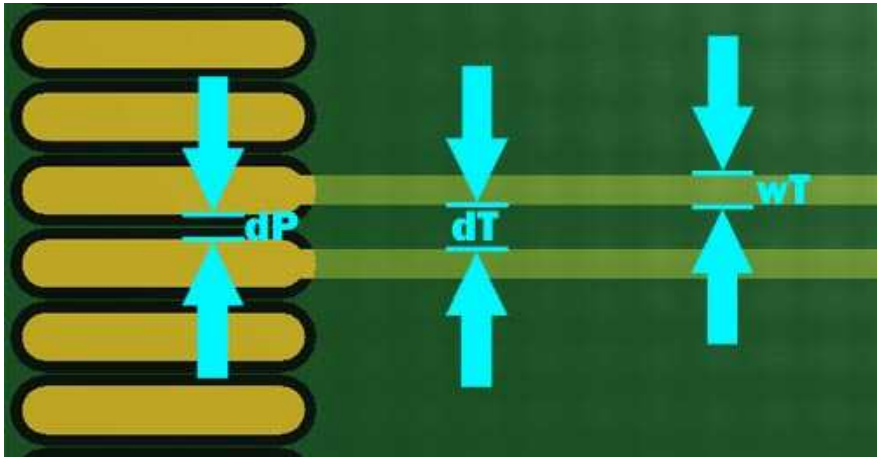
[2]



[2]

Important Terminology

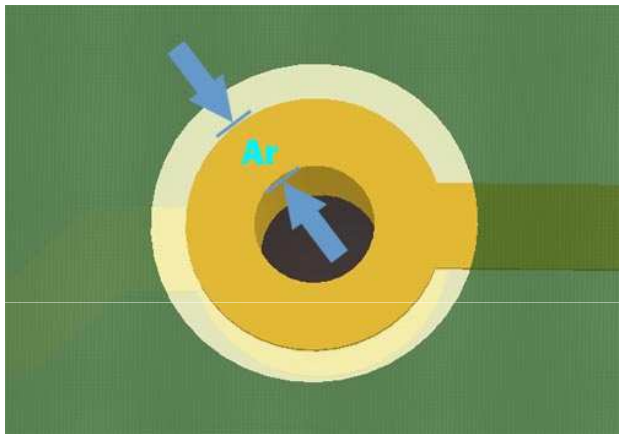
- Trace
  - The width of a metal wire
- Space
  - The minimum distance between traces
- “Trace/Space”
  - “6 mil trace/space” means the traces must be at least 6 mils wide and there must be at least 6 mils of space between traces



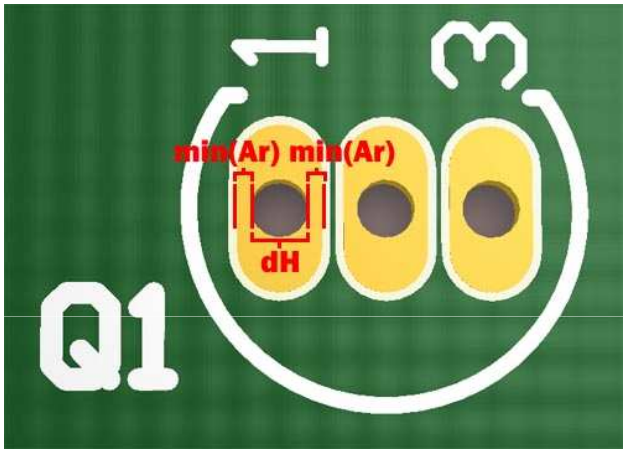
[1]

Important Terminology

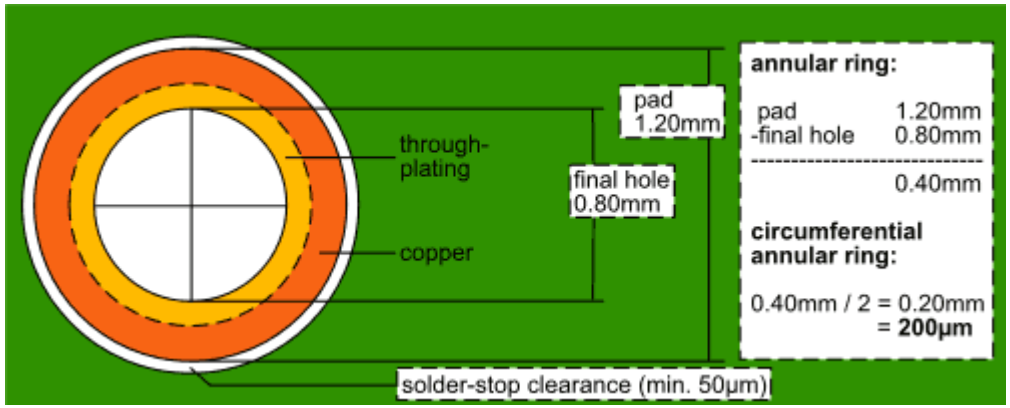
- Pad
  - Surface mount (SM) and/or with hole



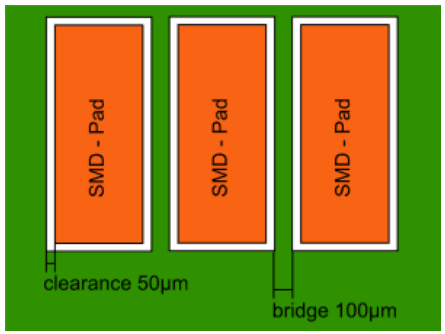
[1]



[1]



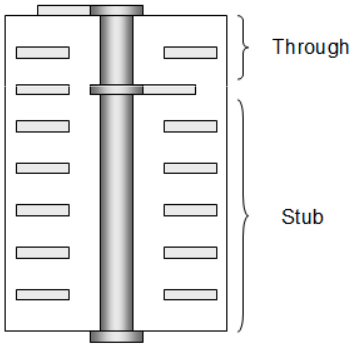
[2]



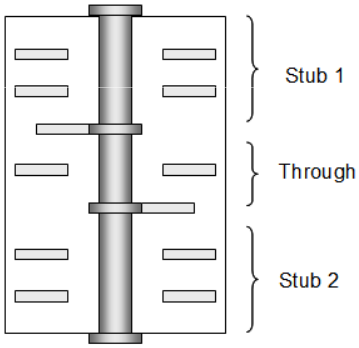
[2]

Important Terminology

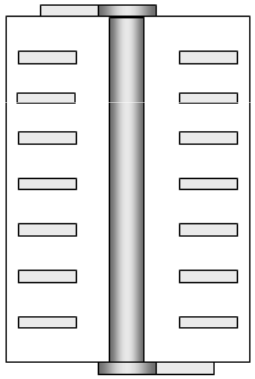
- Via
  - A ‘via’ is a metal-plated hole drilled in the PCB that connects metal layers
  - Four common types are ‘stub’, ‘through-hole’, ‘blind’, and ‘buried’
  - Figures are from [3]

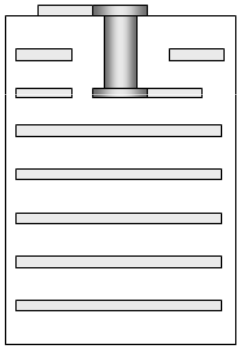


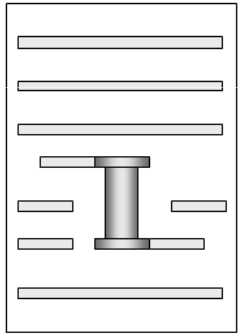
Stub Via A



Stub Via B


Through


Blind Via


Buried Via

Advanced Circuits (AC) Specials

- These selections will depend on your design needs.
- If interested in the $33 or $66 specials, be sure to adjust settings appropriately

Full Spec 2-Layer Designs Only $33 Each!

To Order Now, Upload Your Zipped Files
Click Here to Upload Files and Place Order

$33 Each Specifications	
Min. qty. 4 Boards	White Legend (1 or 2 sides)
Lead Time 5 Days	1 Part Number Per Order (extra $50 charge for multiple parts or step & repeat)
2-Layers, FR-4, 0.062", 1 oz. cu. plate	Max. size 60 sq. inches
Lead FREE Solder Finish	No slots (or overlapping drill hits)
Min. 0.006" line/space	No Internal routing (cutouts)
Min. 0.015" hole size	No scoring, tab rout or drilled hole board separations
All Holes Plated	Routed to overall dimensions
Green LPI Mask	Maximum 35 drilled holes Per Sq. Inch

Credit Card orders only please.

Full Spec 4-Layer Designs Only $66 Each!

To Order Now, Upload Your Zip Files

Click Here to Upload Files and Place Order

$66 Each Specific	
Min. Qty 4 Boards	White Legend (1 or 2 sides)
Lead Time 5 Days	1 Part Number per Order (extra $50 charge for multiple parts or step & repeat)
4-Layers, FR-4, 0.062" 1 oz. cu plate	Max. Size 30 sq. inches
Lead FREE Solder Finish	No Slots (or overlapping drill hits)
Min. 0.006" line/space	No Internal Routing (cutouts)
Min. 0.015" hole size	No Scoring, tab rout, or drilled hole board separations
All Holes Plated	Routed to overall dimensions
Maximum 35 drilled holes per sq. inch	Green LPI Mask

Credit Card orders only please. Does Not Include Blind/Buried Vias.

AC Capabilities

Mechanical Capabilities	
Machining Drill Capabilities	
Primary Drilled Hole Location Tolerance to Datum (Hole) Zero (DTP)	.005"
2nd Drill Hole Location Tolerance to Datum Zero (DTP)	.005"
Minimum Clearance from Copper Conductor to Mechanical Drilled Hole	.007"
Plated Through Hole Capabilities	
Smallest Plated Thru Hole Size: (Finished Via Size with Finished Hole Size – 1 mil Min. Ave. Copper Requirement)	
Finished Panel Thickness .062"	.006" Drill .003" Finished
Plated Hole Tolerance	+/- .002"
Plated hole Spacing Minimum (Drilled hole to hole)	.007"
Pad Diameter to Finished Hole Size	
Conventional Drilling	Drill size plus .015"
Minimum Pad / Drill / Plated Hole	Drill size plus .008"
(Pad Size for Tangency. Add 2X minimum annular ring as needed)	PAD / DRILL / HOLE
.062 Thick Board	.014" / .006" / .003"

AC Tolerances

Inner Layer Clearances

We require a minimum of 0.010" inner layer clearance.

Copper to Edge of Printed Circuit Board

Minimum of 0.010" (outer layers) and 0.015" for inner layers (0.020" preferred for inner layers). For scoring, minimum of .015 for outer layers and .020 for inner layers.

Pad Size/Annular Ring

Pad size should be at least + 0.010" over finished hole size for vias and + 0.014" over finished hole size for component holes. This means the annular ring (radius of the pad) should be at least .005" for vias and a minimum of 0.007" for component holes.

Hole Size

+/- 0.005" Standard Spec (applies to holes up to .250", larger holes will be routed, see Rout tolerances below)

Copper Trace Width/Spacing (Trace and space)

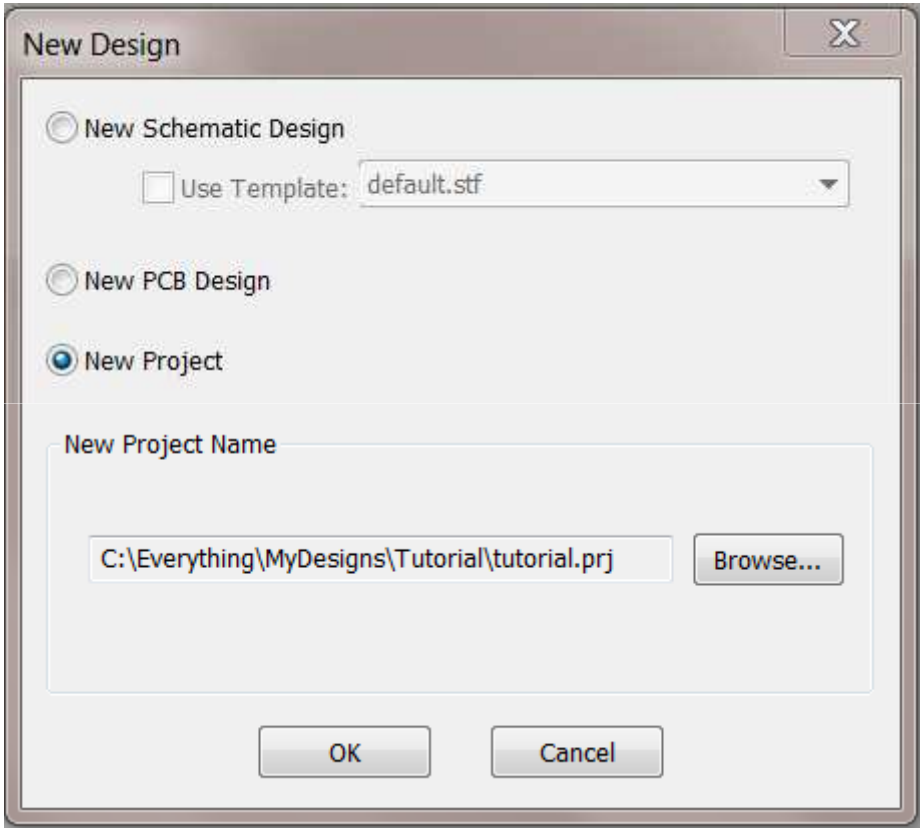
Copper spacing is the minimum air gap between any two adjacent copper features. Trace width is the minimum width of a copper feature, usually traces.

Requirements: A premium is charged for trace width/spacing less than .007".
(We can process .004" for 1 oz. CU. finished (outer layers) and .5 oz. CU finished (inner layers).
For 1 oz. finished copper weight (inner layers), the minimum trace width/space is 0.005"
For 2 oz. finished copper weight (inner & outer), the minimum trace width/space is 0.006"

PCB Artist

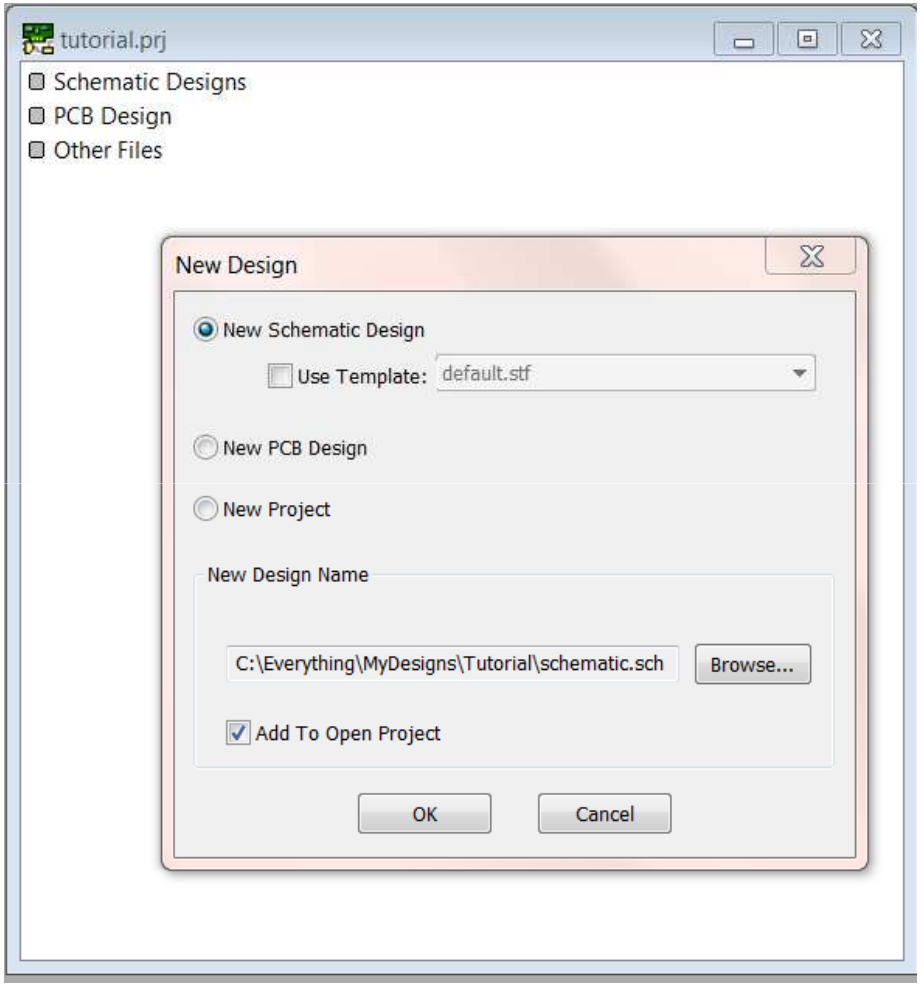
New Project

- File->New
- Select New Project and specify path for *.prj file



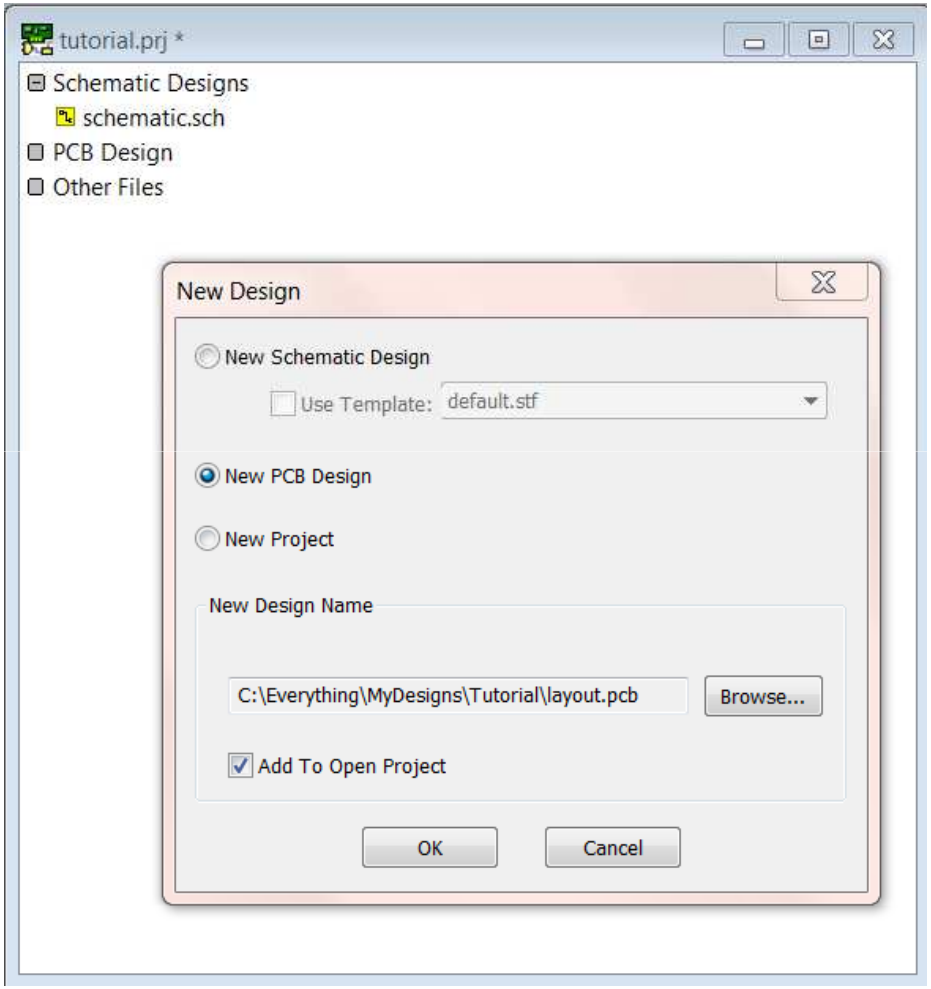
Add Schematic

- File->New
- Select New Schematic, assign file name and check Add to Open Project



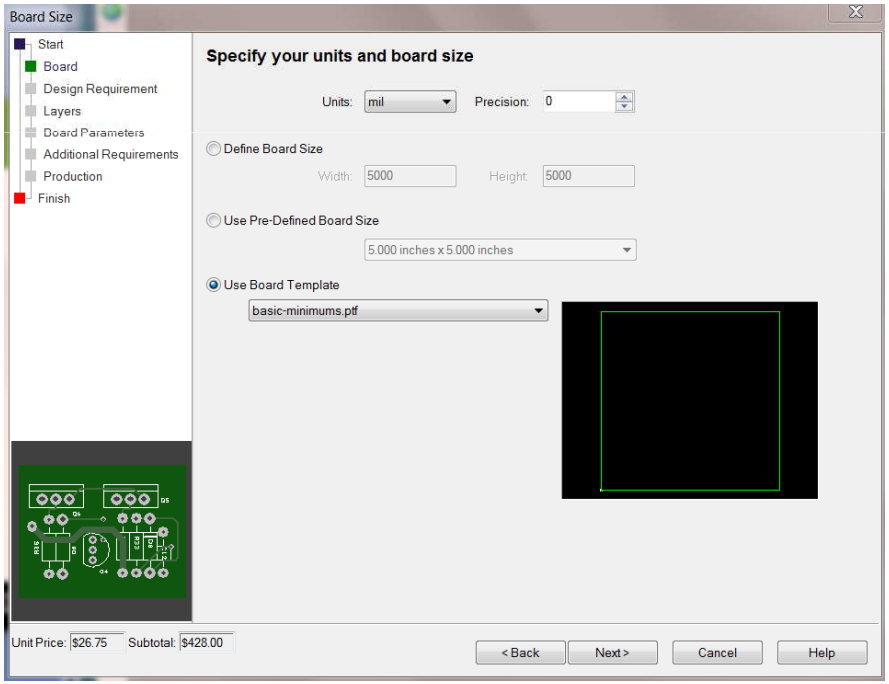
Add PCB Layout

- File->New
- Select New PCB Design, assign file name and check Add to Open Project
- Selecting OK will launch the PCB Wizard



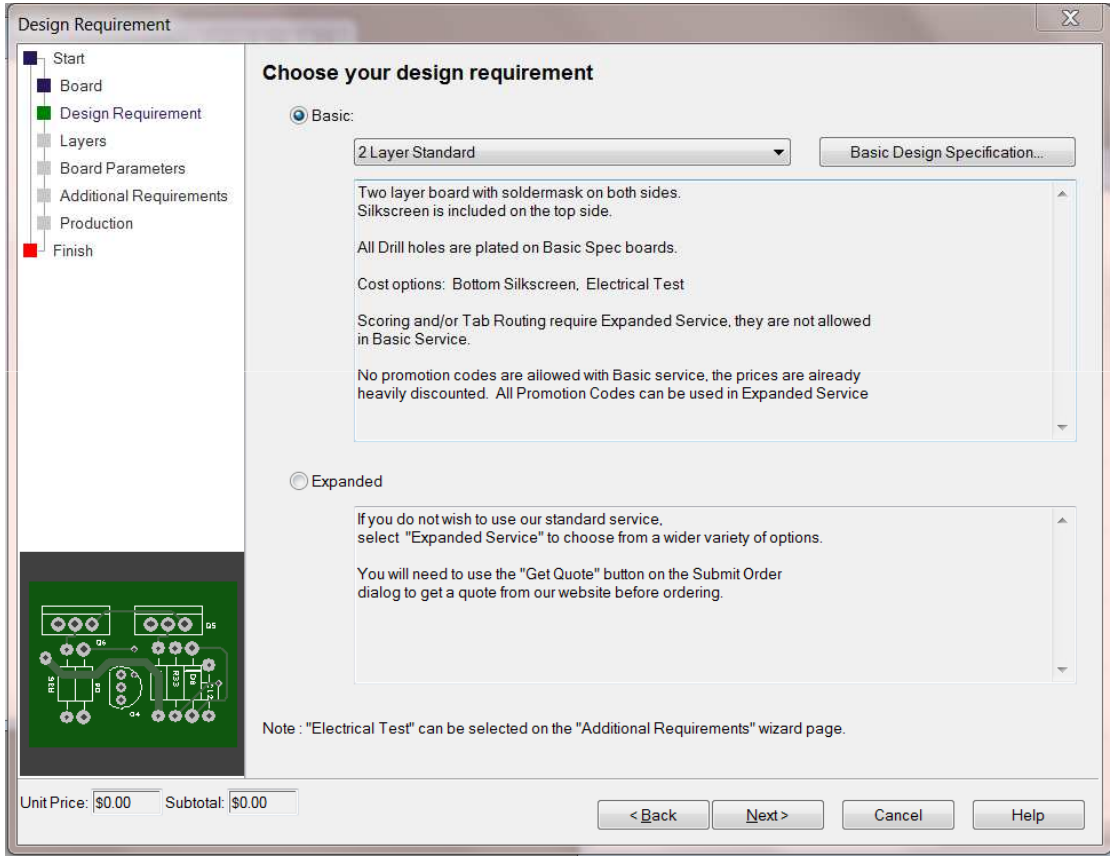
PCB Wizard

- Set units to “mils” and precision to “0”
  - Precision is the number of places to the right of the decimal
  - A value of “1” allows for measurements such as 15.8mils, but not 15.75mils. For 15.75mils, precision should be set to “2”
  - Use ‘basic-minimums’ for board template



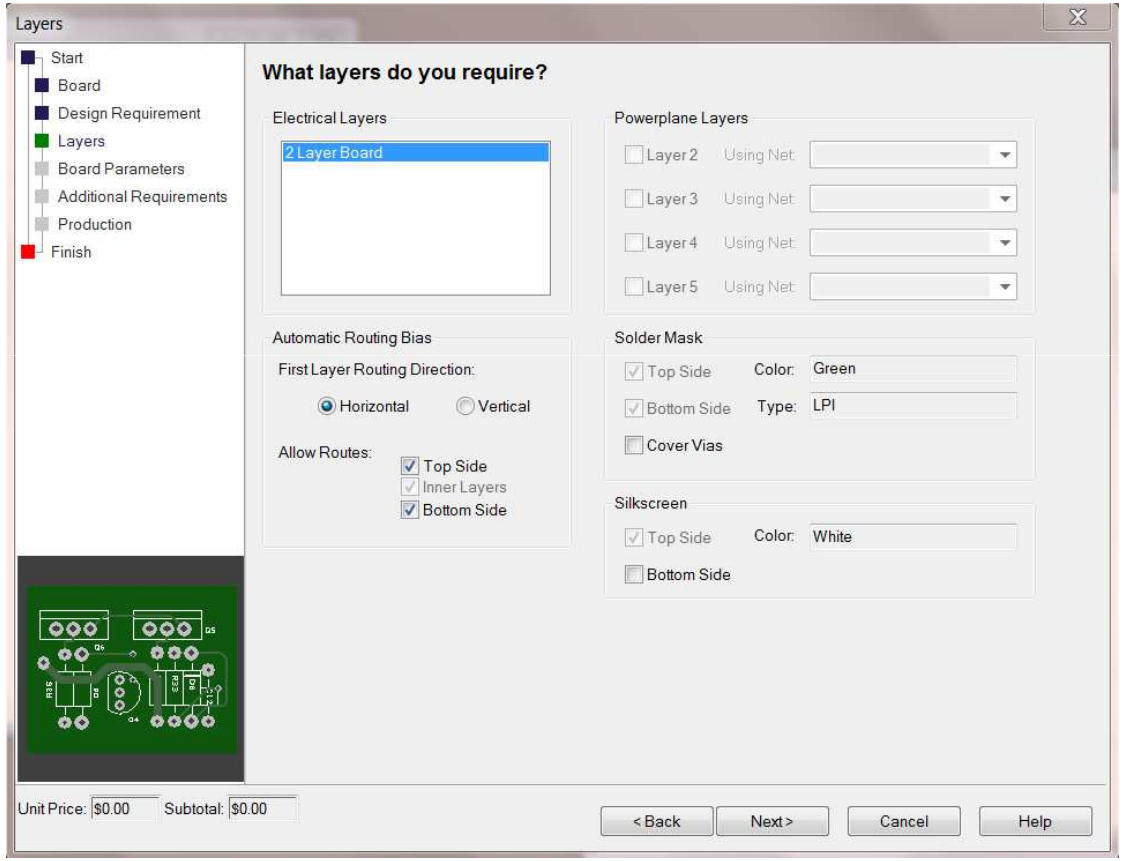
PCB Wizard

- Select appropriate board service (most will probably be 2 or 4 layer standard)



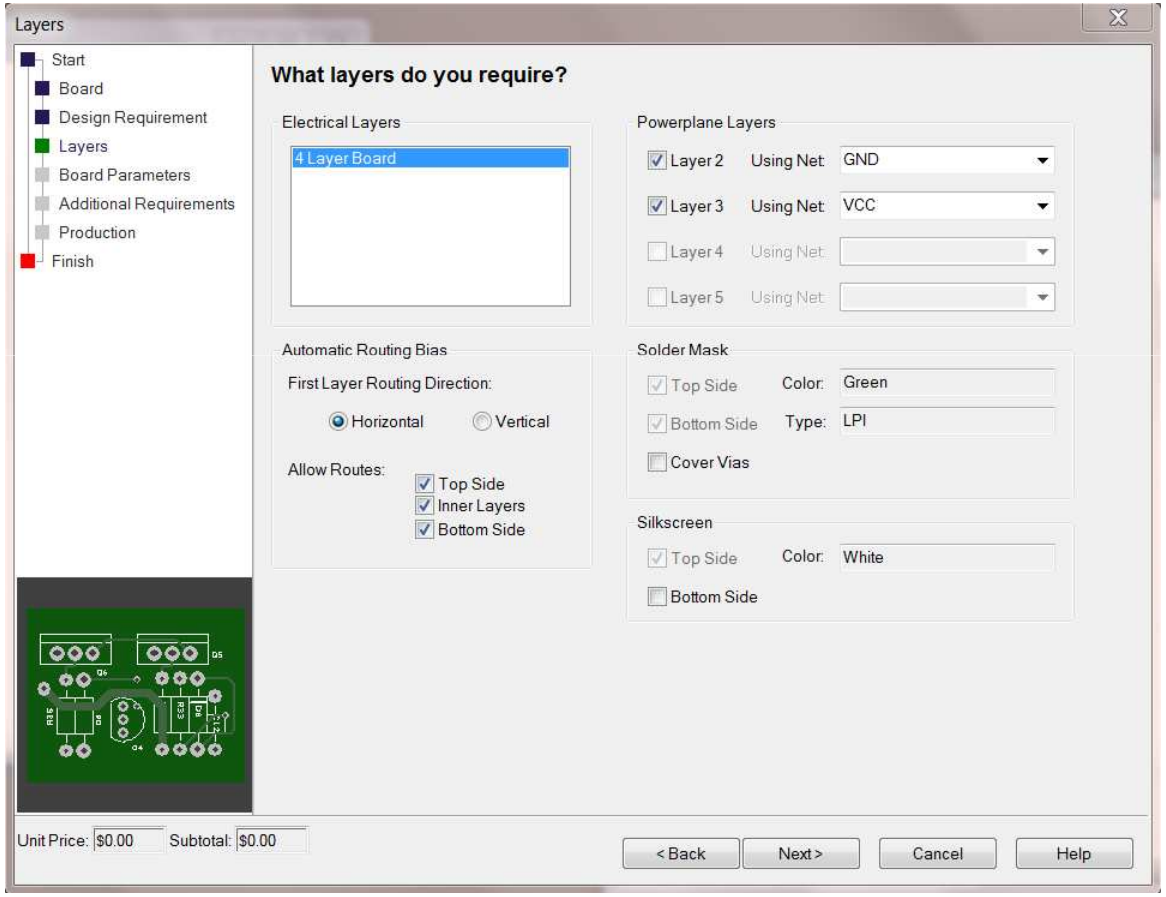
PCB Wizard

- For a 2-layer board the parameters will be straightforward

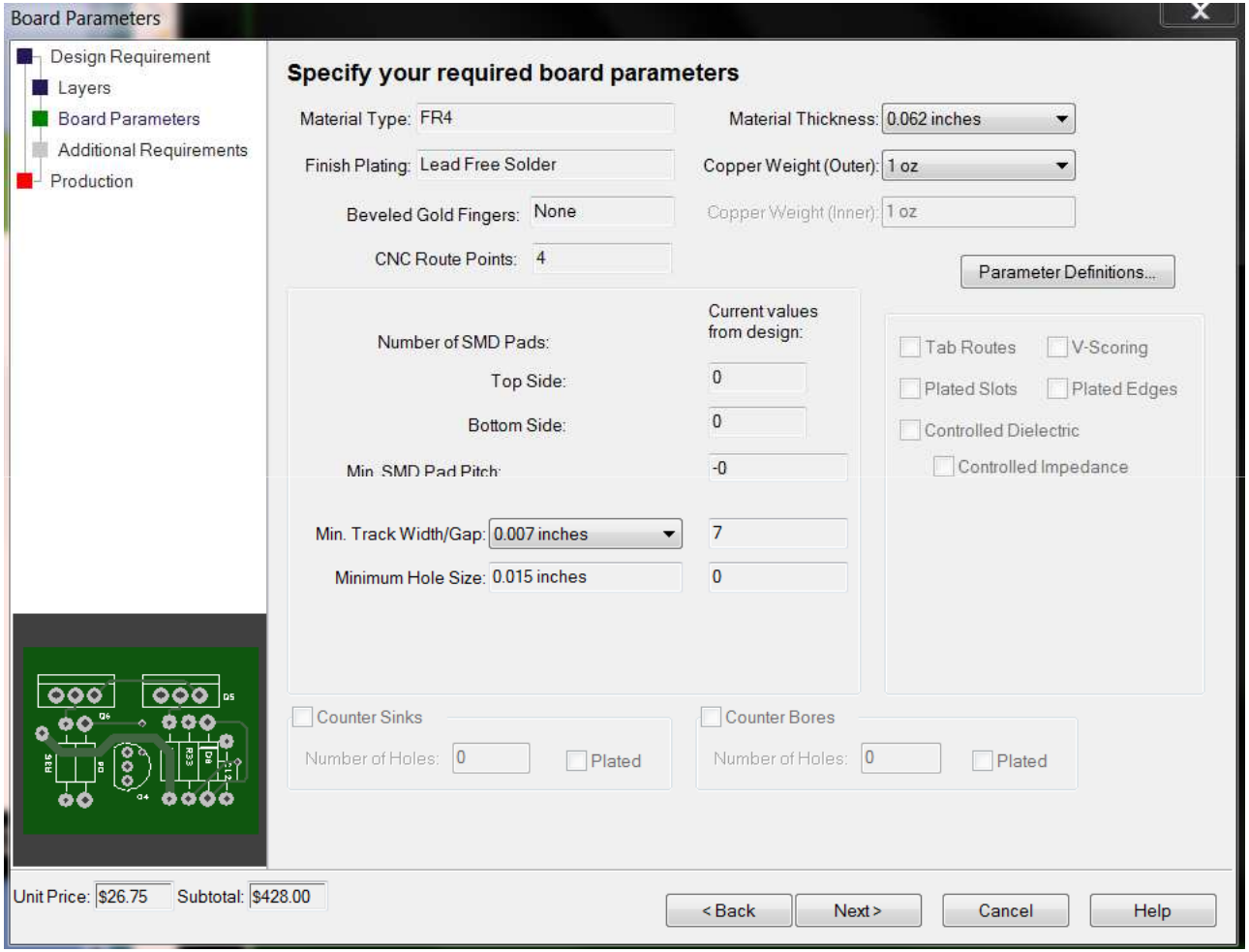


PCB Wizard

- For a 4-layer board you can specify powerplane layers

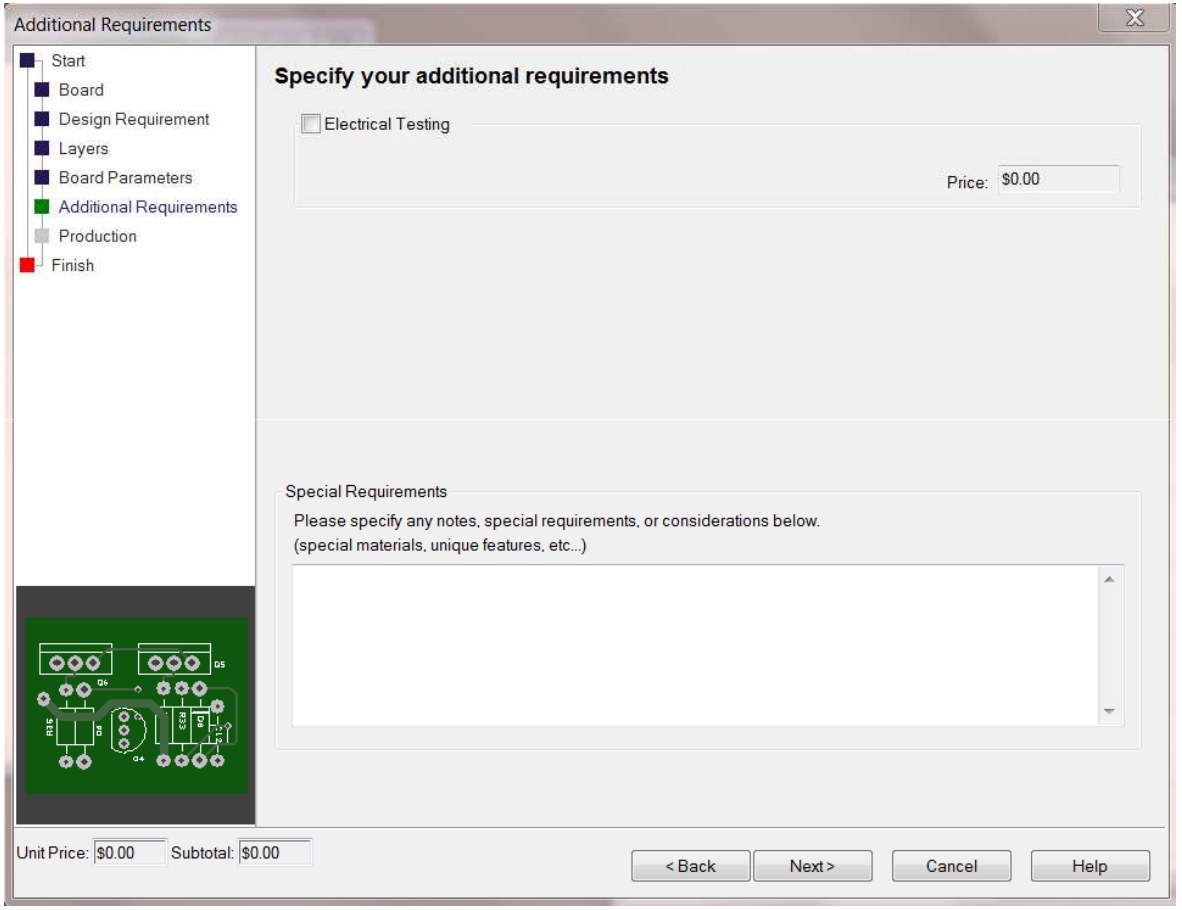


PCB Wizard


Board Parameters
Design Requirement
Layers
Board Parameters
Additional Requirements
Production
Specify your required board parameters
Material Type: FR4
Material Thickness: 0.062 inches
Finish Plating: Lead Free Solder
Copper Weight (Outer): 1 oz
Beveled Gold Fingers: None
Copper Weight (Inner): 1 oz
CNC Route Points: 4
Parameter Definitions...
Current values from design:
Number of SMD Pads:
Top Side: 0
Bottom Side: 0
Min. SMD Pad Pitch: -0
Tab Routes
V-Scoring
Plated Slots
Plated Edges
Controlled Dielectric
Controlled Impedance
Min. Track Width/Gap: 0.007 inches 7
Minimum Hole Size: 0.015 inches 0
Counter Sinks
Number of Holes: 0
Plated
Counter Bores
Number of Holes: 0
Plated
Unit Price: $26.75
Subtotal: $428.00
< Back
Next >
Cancel
Help

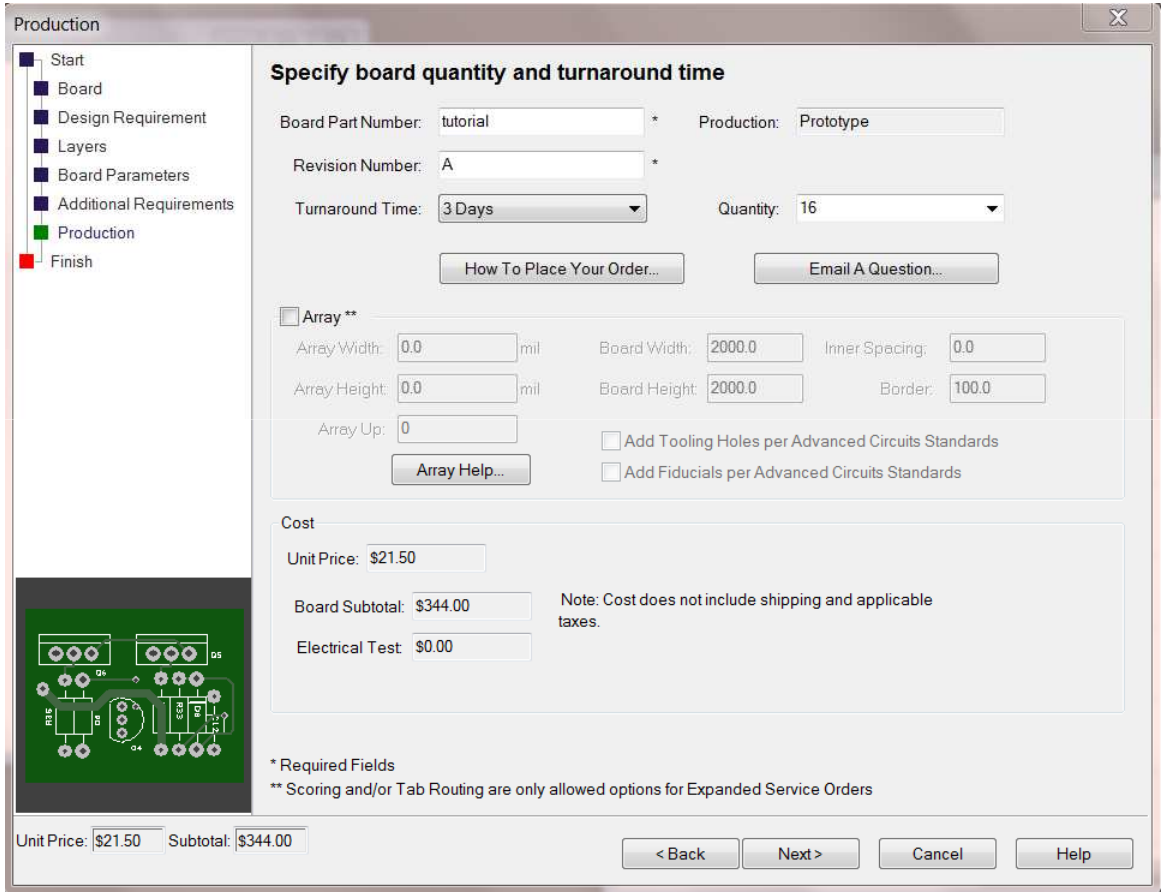
PCB Wizard

- Select whether or not you want electrical testing (probably not)



PCB Wizard

- Specify board part number, revision, and quantity
- Adjust turnaround time as needed
  - 3 days is recommended
- Select Next, then Finish.

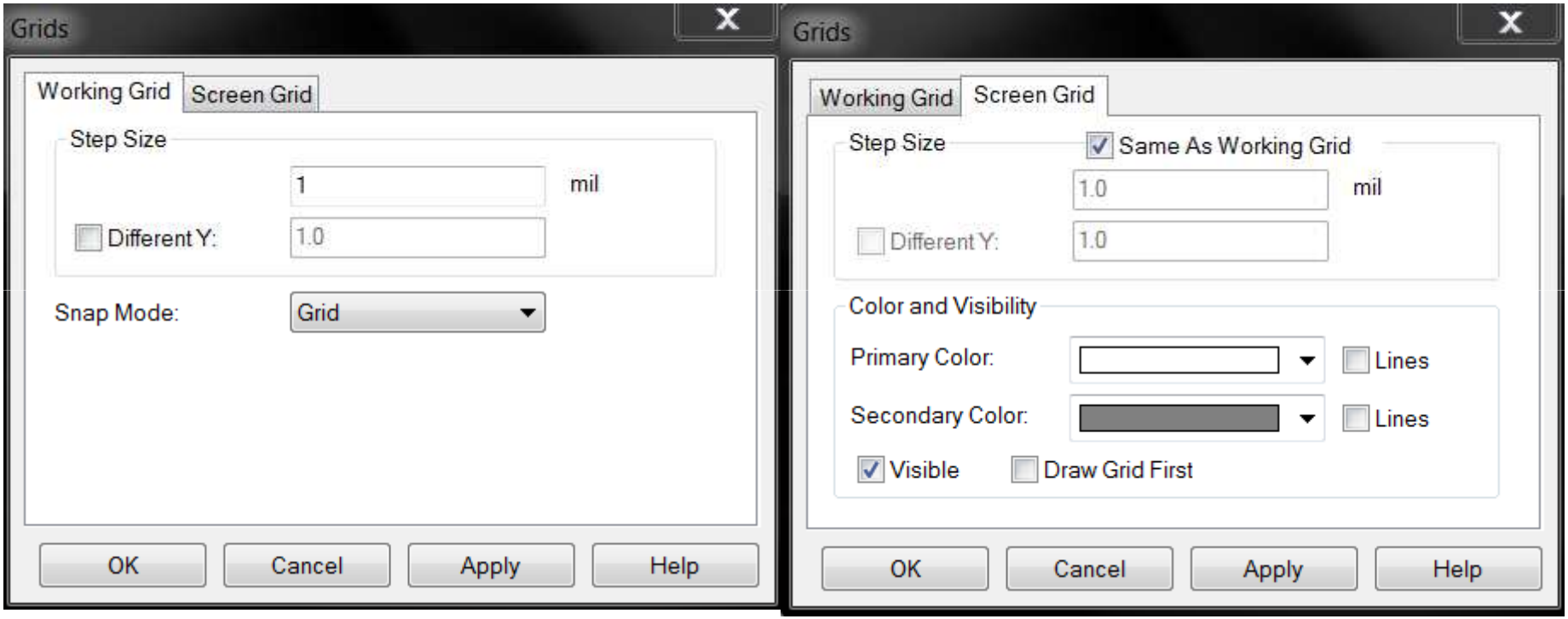


PCB Settings

- Grid
- Units
- Styles
- Spacings
- Nets
- Net Classes

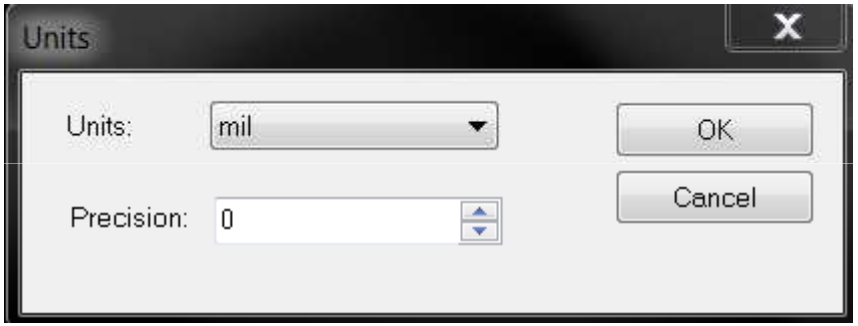
PCB Settings-Grid

- Settings->Grids



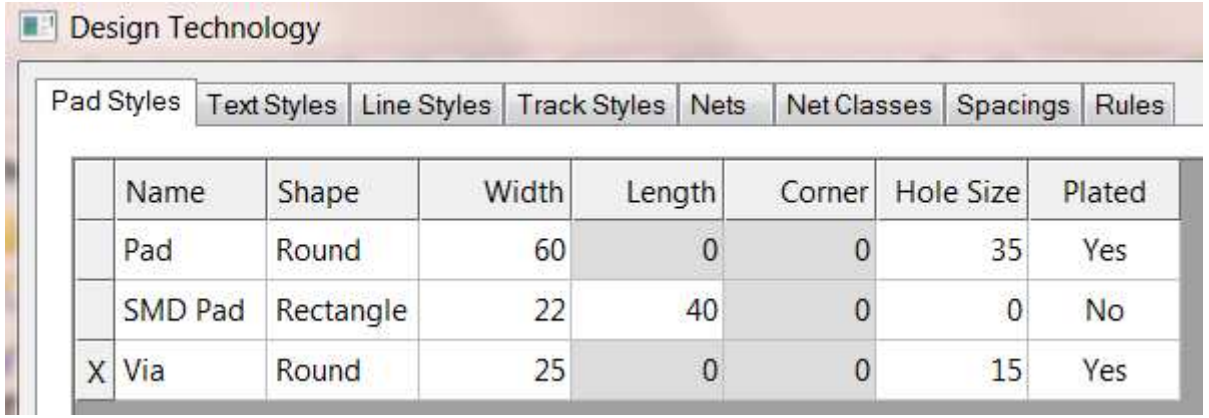
PCB Settings-Units

- Settings->Units

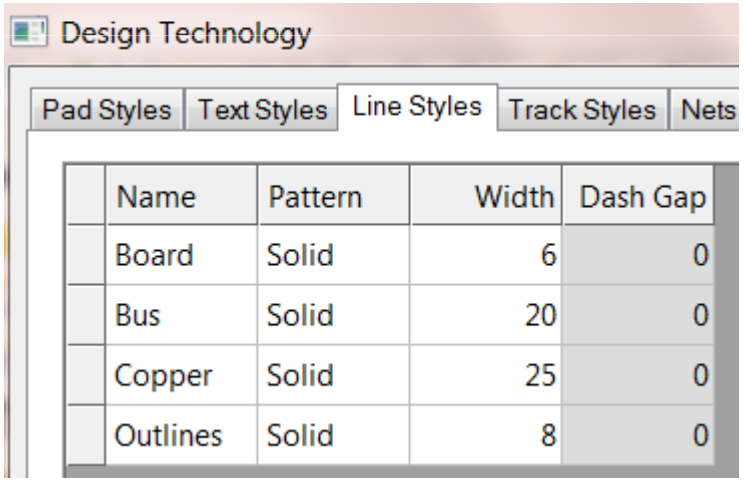


PCB Settings-Styles

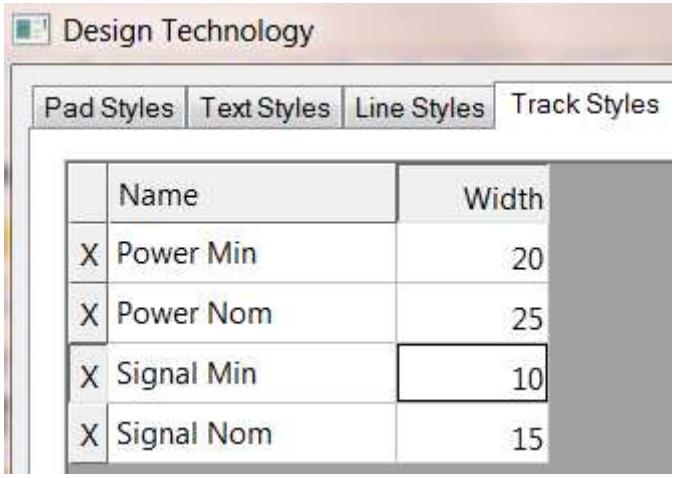
- Settings->Styles



	Name	Shape	Width	Length	Corner	Hole Size	Plated
	Pad	Round	60	0	0	35	Yes
	SMD Pad	Rectangle	22	40	0	0	No
X	Via	Round	25	0	0	15	Yes



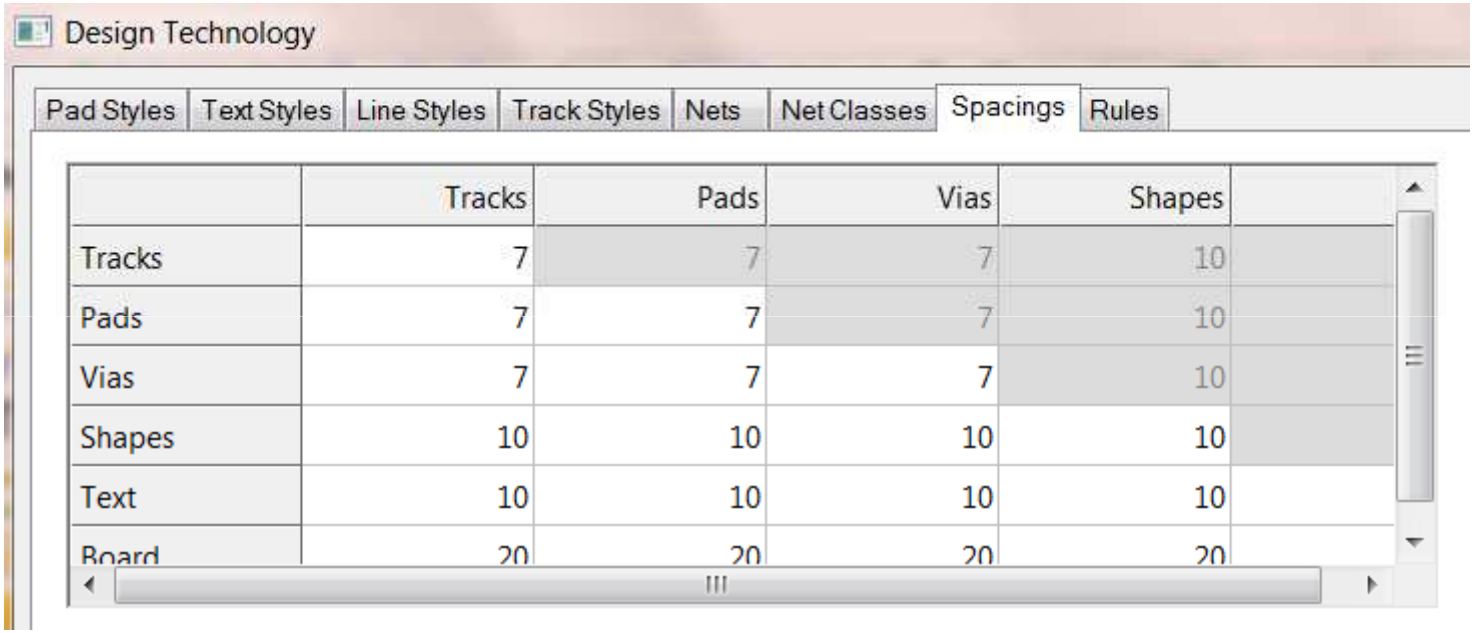
	Name	Pattern	Width	Dash Gap
	Board	Solid	6	0
	Bus	Solid	20	0
	Copper	Solid	25	0
	Outlines	Solid	8	0



	Name	Width
X	Power Min	20
X	Power Nom	25
X	Signal Min	10
X	Signal Nom	15

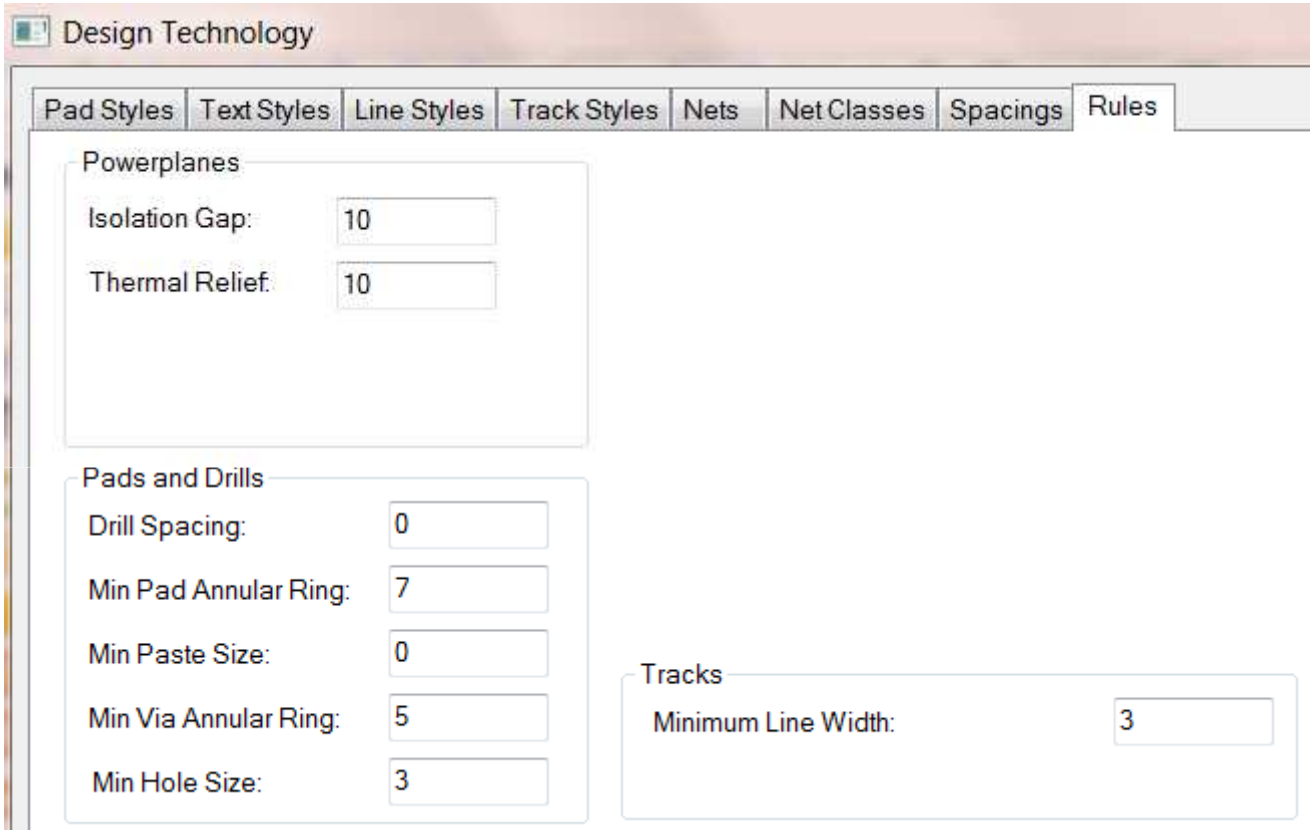
PCB Settings-Spacings

- Settings->Spacings

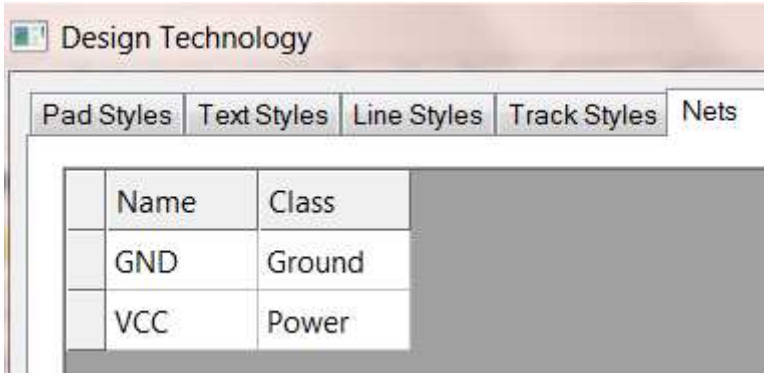


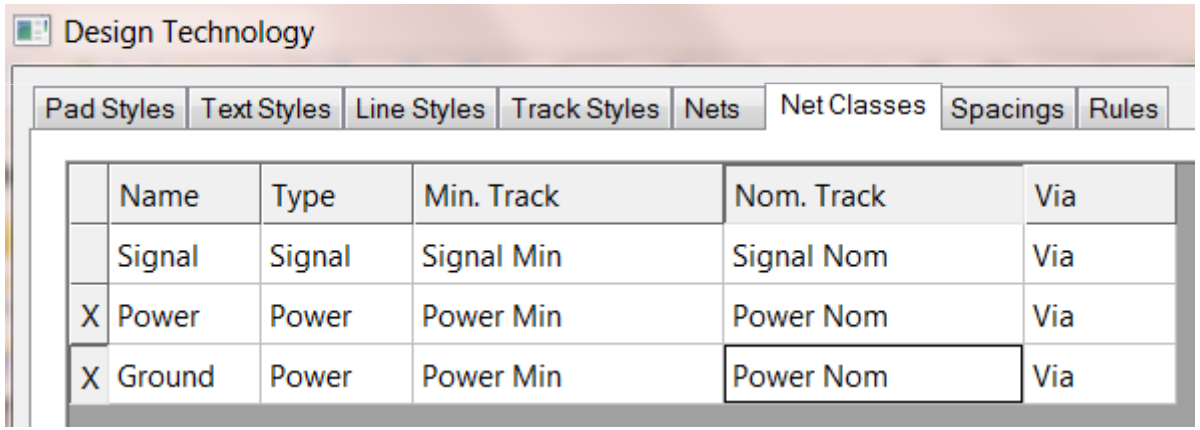
	Tracks	Pads	Vias	Shapes
Tracks	7	7	7	10
Pads	7	7	7	10
Vias	7	7	7	10
Shapes	10	10	10	10
Text	10	10	10	10
Board	20	20	20	20

PCB Settings-Rules



PCB Settings-Nets & Net Classes

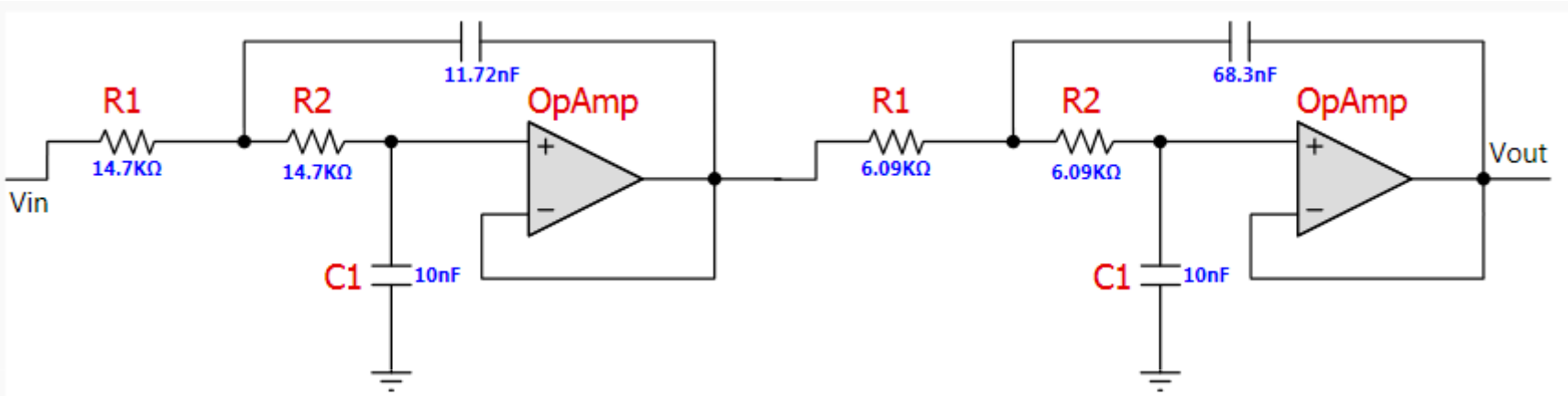




Example Design

- Let’s create the schematic and PCB for the following filter
  - Active low-pass
  - Fc=1kHz
  - 4^{th} order
  - 2-stage
  - Sallen-Key
- We can use TI’s FilterPro to obtain a generic schematic
- Then use TI’s TINA-TI to verify in simulation

FilterPro Design



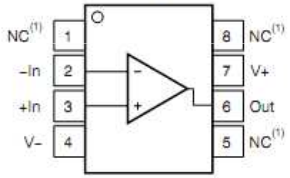
Filter Stage:	1	Filter Stage:	2
Passband Gain(Ao):	1	Passband Gain(Ao):	1
Cutoff Frequency(fn):	1 kHz	Cutoff Frequency(fn):	1 kHz
QualityFactor (Q):	0.54	QualityFactor (Q):	1.31
Filter Response:	Butterworth	Filter Response:	Butterworth
Circuit Topology:	SallenKey	Circuit Topology:	SallenKey

Amplifier Selection

- Let’s implement this filter with the OPA141
  - Single-supply, 10MHz, RRO, Low-noise, JFET input (Ib=20pA max)
  - Supply: 4.5V to 36V
  - Packages
    - Single (SO-8, MSOP-8)
    - Dual (SO-8, MSOP-8)
    - Quad (TSSOP-14, SO-14)
  - Vicm includes GND

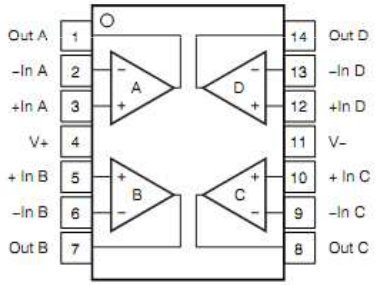
PIN ASSIGNMENTS

OPA141
SO-8, MSOP-8
(TOP VIEW)

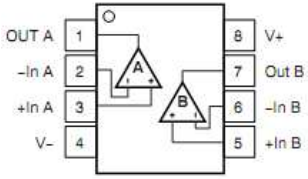


(1) NC denotes no internal connection.

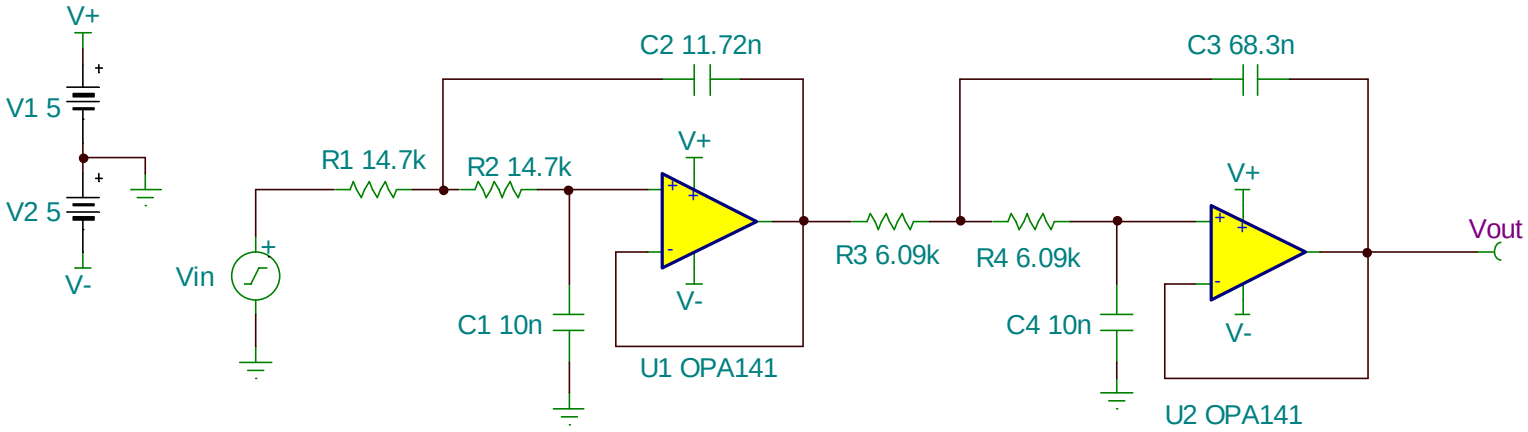
OPA4141
SO-14, TSSOP-14
(TOP VIEW)

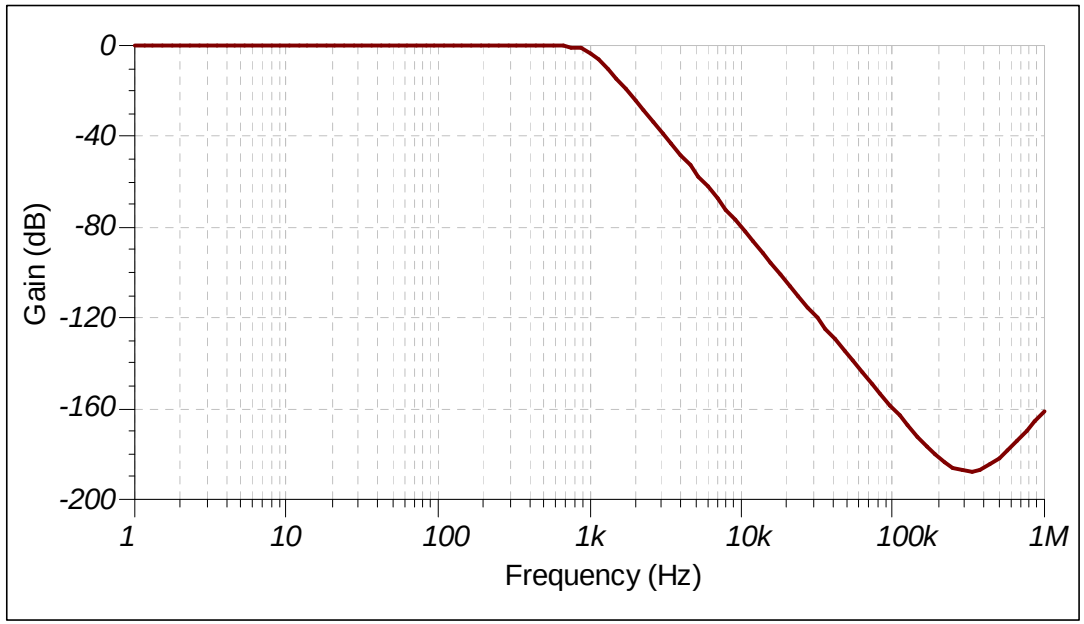


OPA2141
SO-8, MSOP-8
(TOP VIEW)



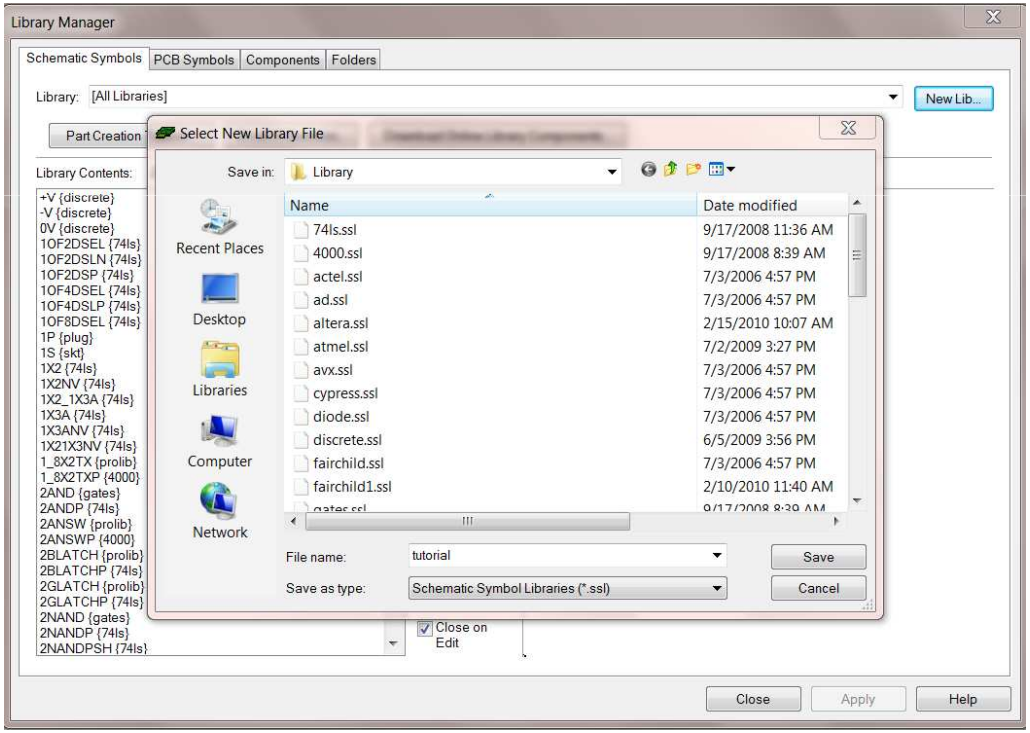
TINA-TI Simulation



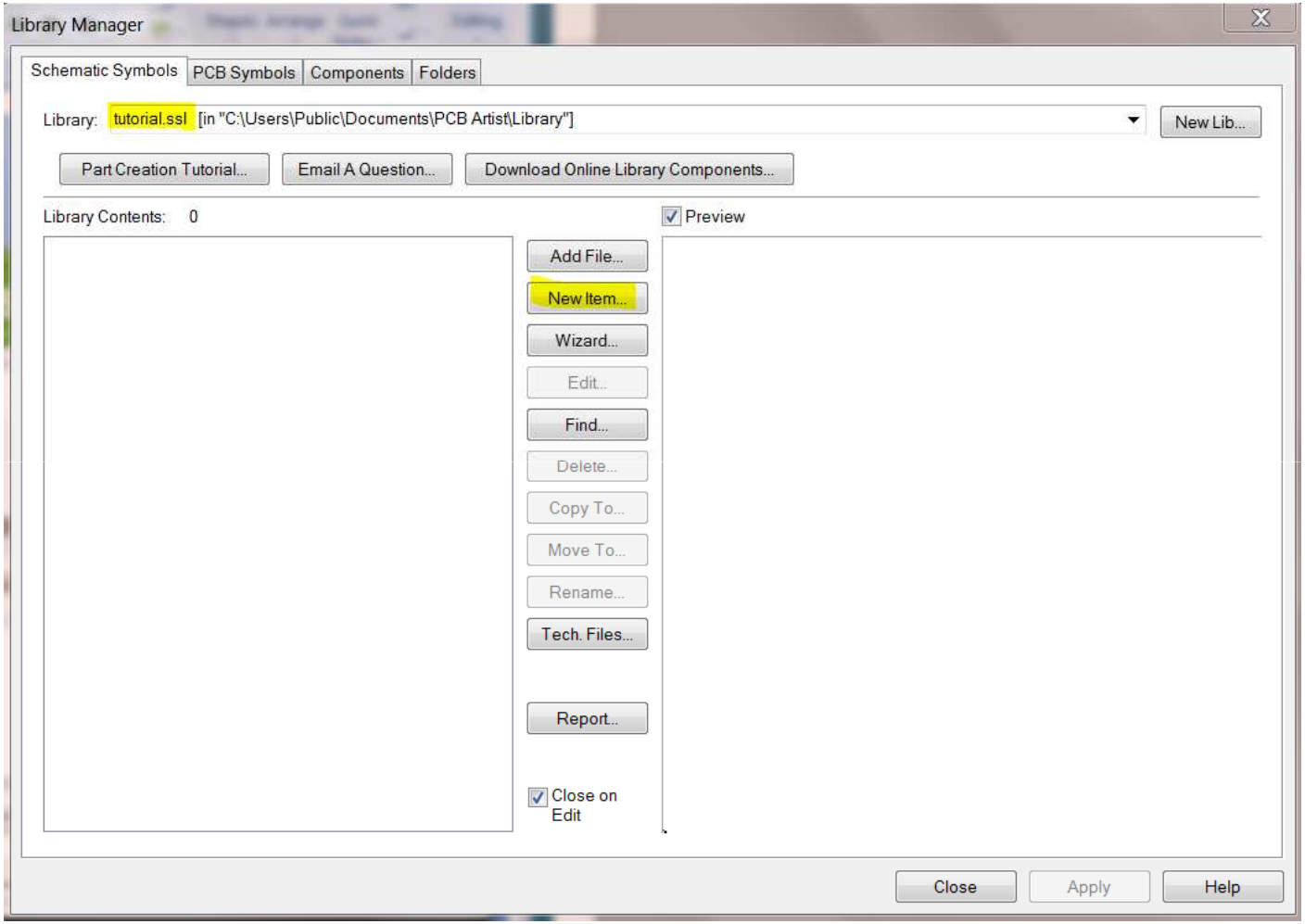


New Schematic Symbol Library

- Let’s create a new Library for custom schematic symbols
  - Open Library Manager (Ctrl-L)
  - Select New Lib
  - Give new library a name

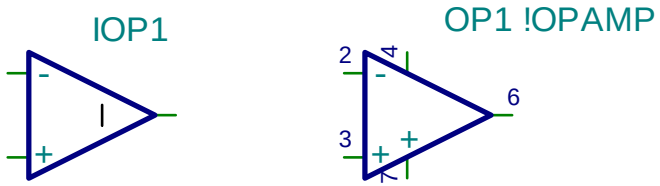


New Schematic Symbol

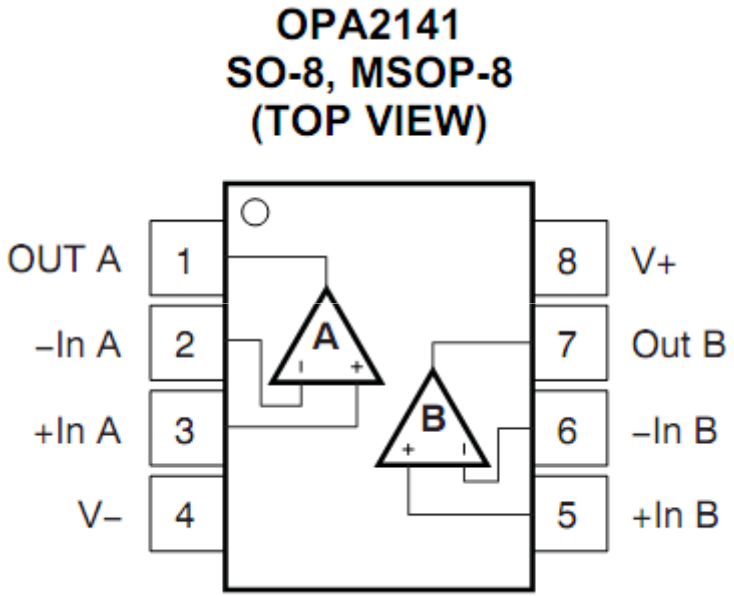


New Schematic Symbol

- For this device we will use the dual version (our filter has 2 amplifiers)
- From a schematic perspective, we will need 2 sub-symbols
  - One will look like an ideal op-amp
  - The second one will have power and ground
  - Here is the idea using symbols from TINA

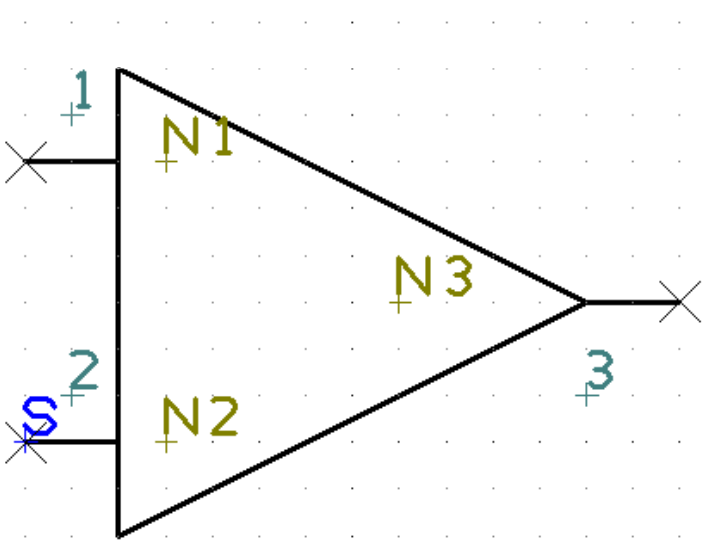


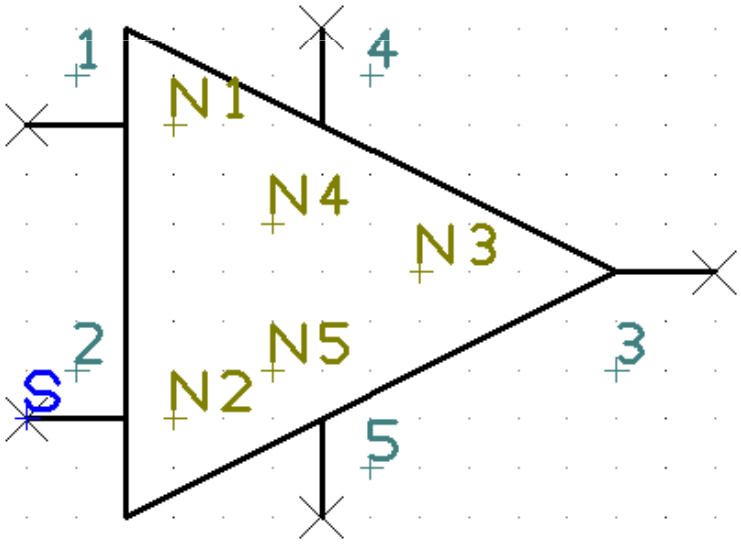
- Note: Please don't use the package pinout as the schematic symbol! This makes it difficult to read the schematic.



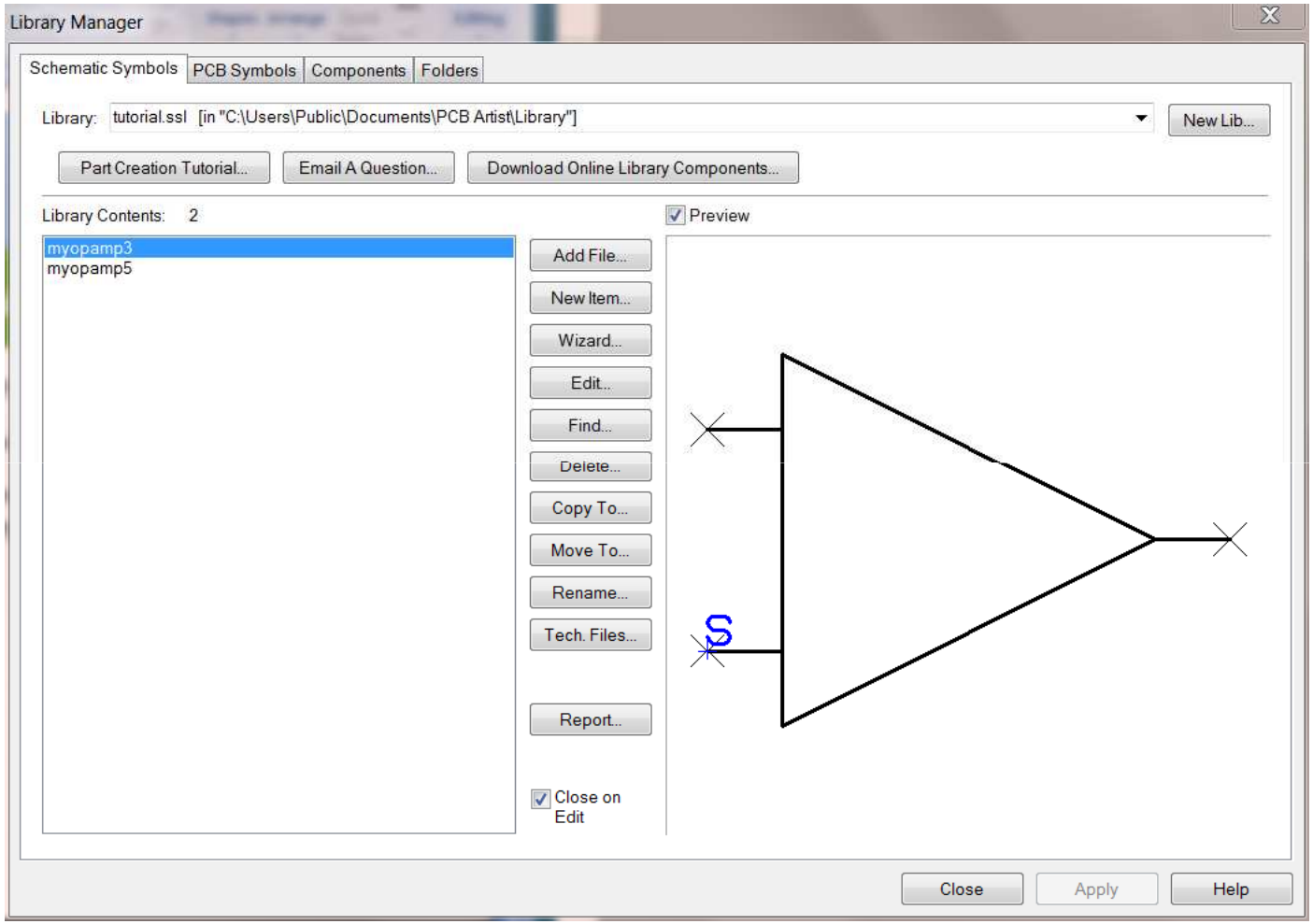
New Schematic Symbol

- Create 2 separate symbols in the library
  - Use “Add Pad” for the pins
  - Use “Single Line” and “Triangle” for the symbol
  - Move the symbol origin (S) to one of the pins
  - The numbers correspond to the pins, “NX” is the pin name
- Save the symbols as myopamp3 and myopamp5



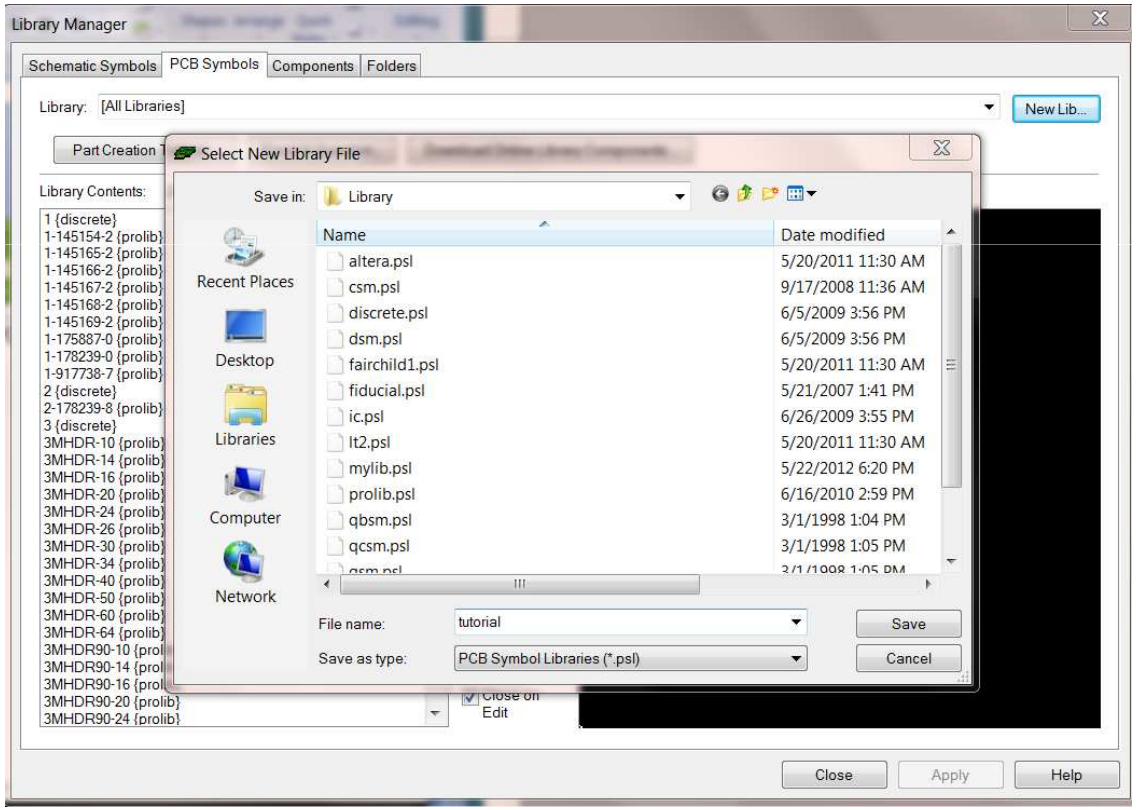


New Schematic Symbol



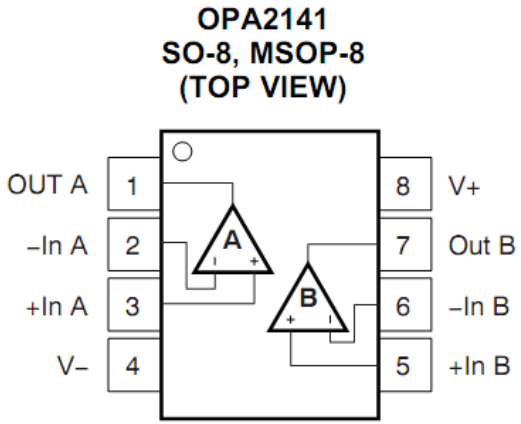
New PCB Symbol Library

- Let’s create a new Library for custom PCB symbols
  - Open Library Manager (Ctrl-L)
  - Select PCB Symbol tab
  - Give new library a name



OPA2141 Packages

- We need to determine which package we will use
- The datasheet typically has all the information required
- We see the OPA2141 comes in two packages
  - MSOP-8
  - SO-8
- TI refers to these packages as “DGK” and “D”



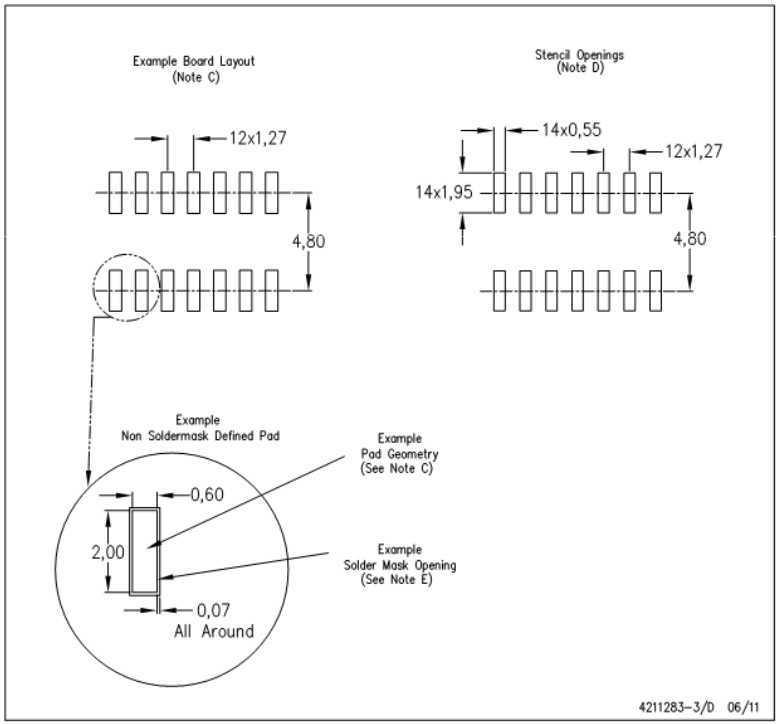
PACKAGE INFORMATION(1)

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	PACKAGE MARKING
OPA141	SO-8	D	O141A
	MSOP-8	DGK	141
OPA2141	SO-8	D	O2141A
	MSOP-8	DGK	2141
OPA4141	TSSOP-14	PW	O4141A
	SO-14	D	O4141AG4

OPA2141 Landing Patterns

- Let’s compare the D and DGK packages
- D is found in the PDS, but DGK is not!
- Here is a link to a useful app note

D (R–PDSO–G14) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

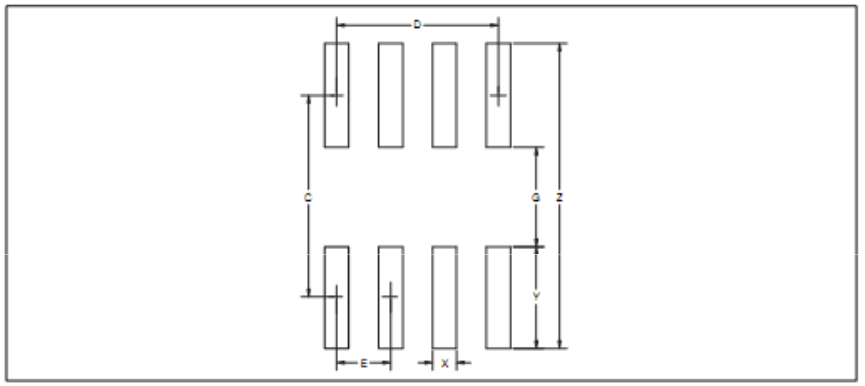


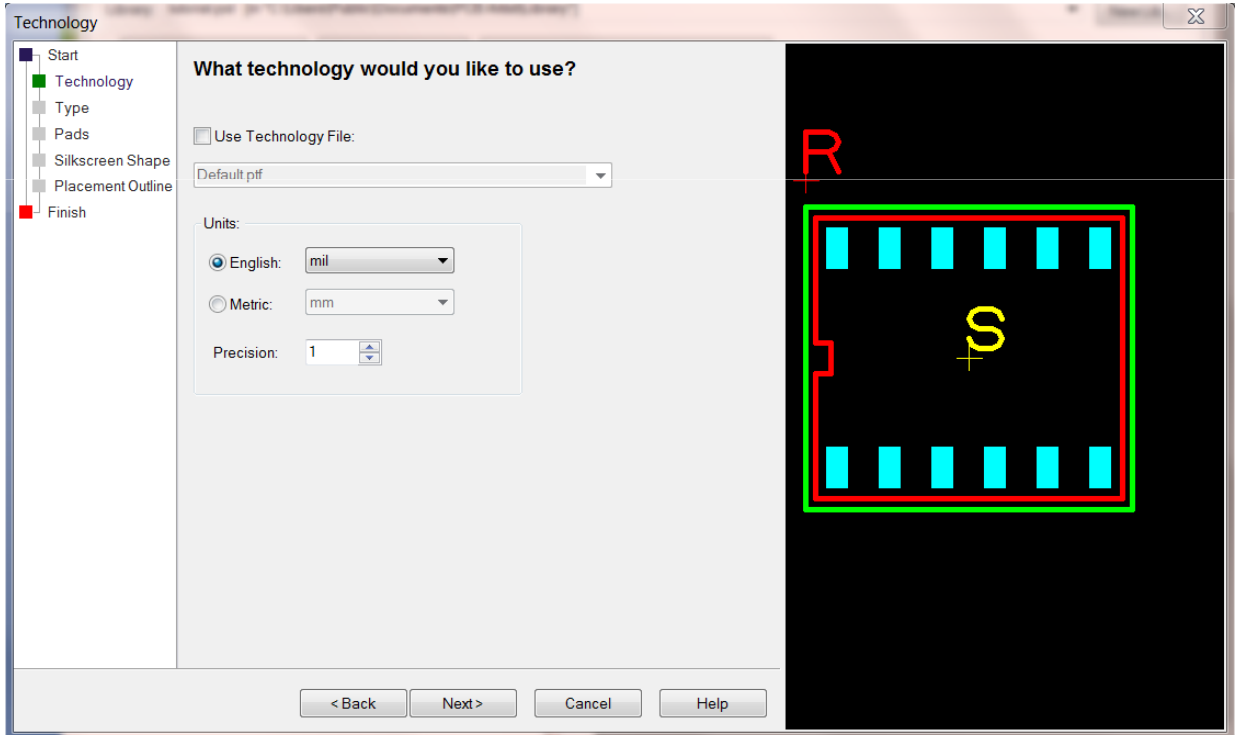
FIGURE 4. Pad Dimensions.

PACKAGE	PKG #	Z MIN	Z MAX	G MIN	G MAX	X MIN	X MAX	Y REF	C/C REF	D REF	E NOM
SO-8	182	0.273	0.277	0.089	0.093	0.018	0.022	0.094	0.183	0.150	0.0500
SO-14	236	0.273	0.277	0.089	0.093	0.018	0.022	0.094	0.183	0.300	0.0500
SO-16	266	0.273	0.277	0.089	0.093	0.018	0.022	0.094	0.183	0.350	0.0500
SO-16W	211	0.447	0.451	0.254	0.258	0.018	0.022	0.099	0.363	0.350	0.0500
SO-18W	219	0.447	0.451	0.254	0.258	0.018	0.022	0.099	0.363	0.400	0.0500
SO-20W	221	0.447	0.451	0.254	0.258	0.018	0.022	0.099	0.363	0.450	0.0500
SO-24W	239	0.447	0.451	0.254	0.258	0.018	0.022	0.099	0.363	0.550	0.0500
SO-28W	217	0.446	0.451	0.278	0.282	0.018	0.022	0.099	0.365	0.650	0.0500
SOT-23-5	331	0.147	0.151	0.034	0.038	0.017	0.021	0.058	0.093	0.075	0.0374
SOT-23-6	332	0.147	0.151	0.034	0.038	0.017	0.021	0.058	0.093	0.075	0.0374
SOT-23-8	348	0.147	0.151	0.015	0.019	0.015	0.020	0.058	0.093	0.077	0.0256
MSOP-8	337	0.226	0.230	0.097	0.101	0.014	0.018	0.058	0.164	0.077	0.0256
SSOP-20	334	0.351	0.355	0.177	0.181	0.013	0.017	0.059	0.266	0.230	0.0256
SSOP-24	338	0.351	0.355	0.177	0.181	0.013	0.017	0.059	0.266	0.281	0.0256
SSOP-28	324	0.351	0.355	0.177	0.181	0.013	0.017	0.059	0.266	0.333	0.0256
SSOP-16	322	0.273	0.277	0.089	0.093	0.011	0.015	0.094	0.183	0.175	0.0250
SSOP-48	333	0.446	0.452	0.276	0.279	0.012	0.016	0.059	0.364	0.575	0.0250
SSOP-56	346	0.446	0.452	0.276	0.279	0.012	0.016	0.059	0.364	0.675	0.0250

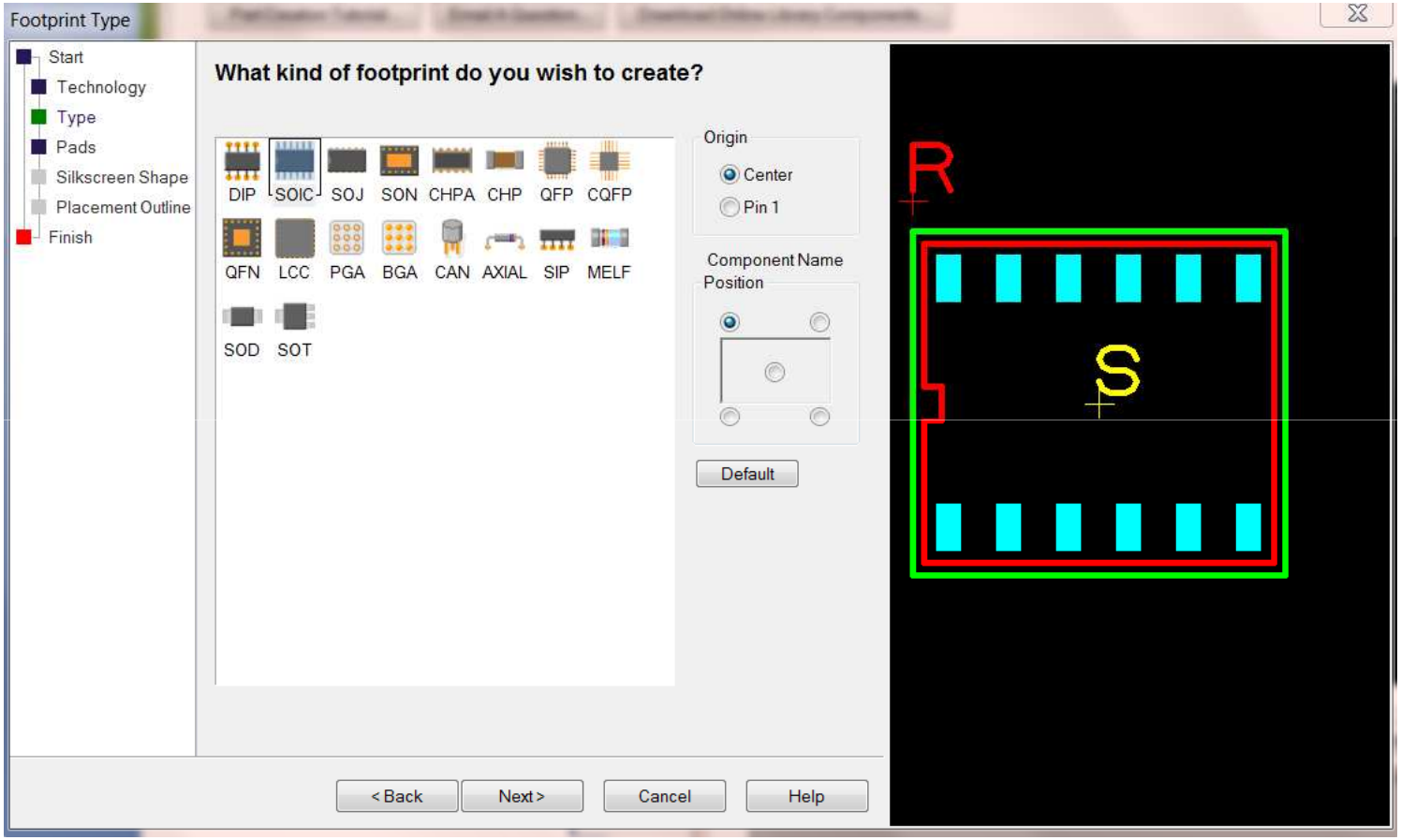
TABLE IV. Pad Dimensions—Inches

New PCB Symbol

- Let’s use the DGK (MSOP-8) for it is smaller
- Create a new Library for custom PCB symbols
  - Open Library Manager (Ctrl-L)
  - Select PCB Symbol tab
  - Give new library a name
  - Let’s use the Wizard
  - Use mils, precision 1

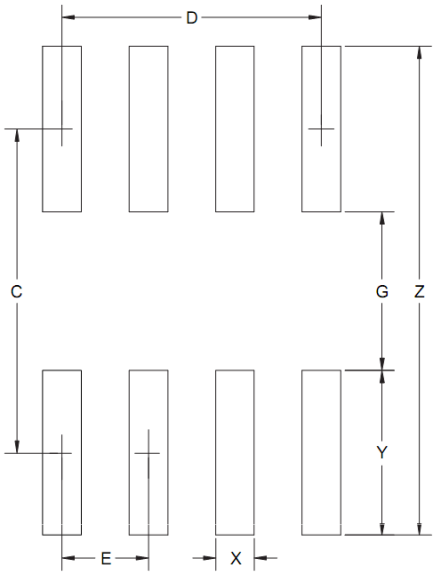


New PCB Symbol



New PCB Symbol

PCB Artist->App Note
*Set H=T=0
e=E=25.6
E=Z=230
L=Y=66
b=X=18



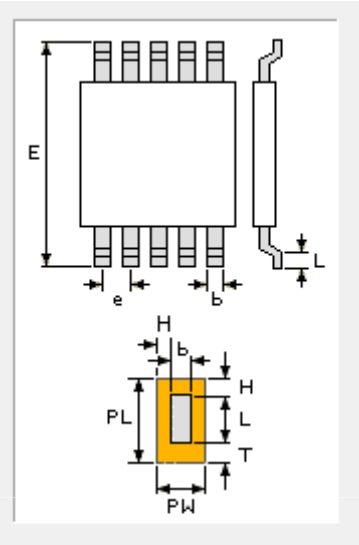


FIGURE 4. Pad Dimensions.

PACKAGE	PKG #	Z MIN	Z MAX	G MIN	G MAX	X MIN	X MAX	Y REF	C/C REF	D REF	E NOM
SO-8	182	0.273	0.277	0.089	0.093	0.018	0.022	0.094	0.183	0.150	0.0500
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SO-16	265	0.273	0.277	0.089	0.093	0.018	0.022	0.094	0.183	0.350	0.0500
SO-16W	211	0.447	0.451	0.254	0.258	0.018	0.022	0.099	0.353	0.350	0.0500
SO-18W	219	0.447	0.451	0.254	0.258	0.018	0.022	0.099	0.353	0.400	0.0500
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SO-24W	239	0.447	0.451	0.254	0.258	0.018	0.022	0.099	0.353	0.550	0.0500
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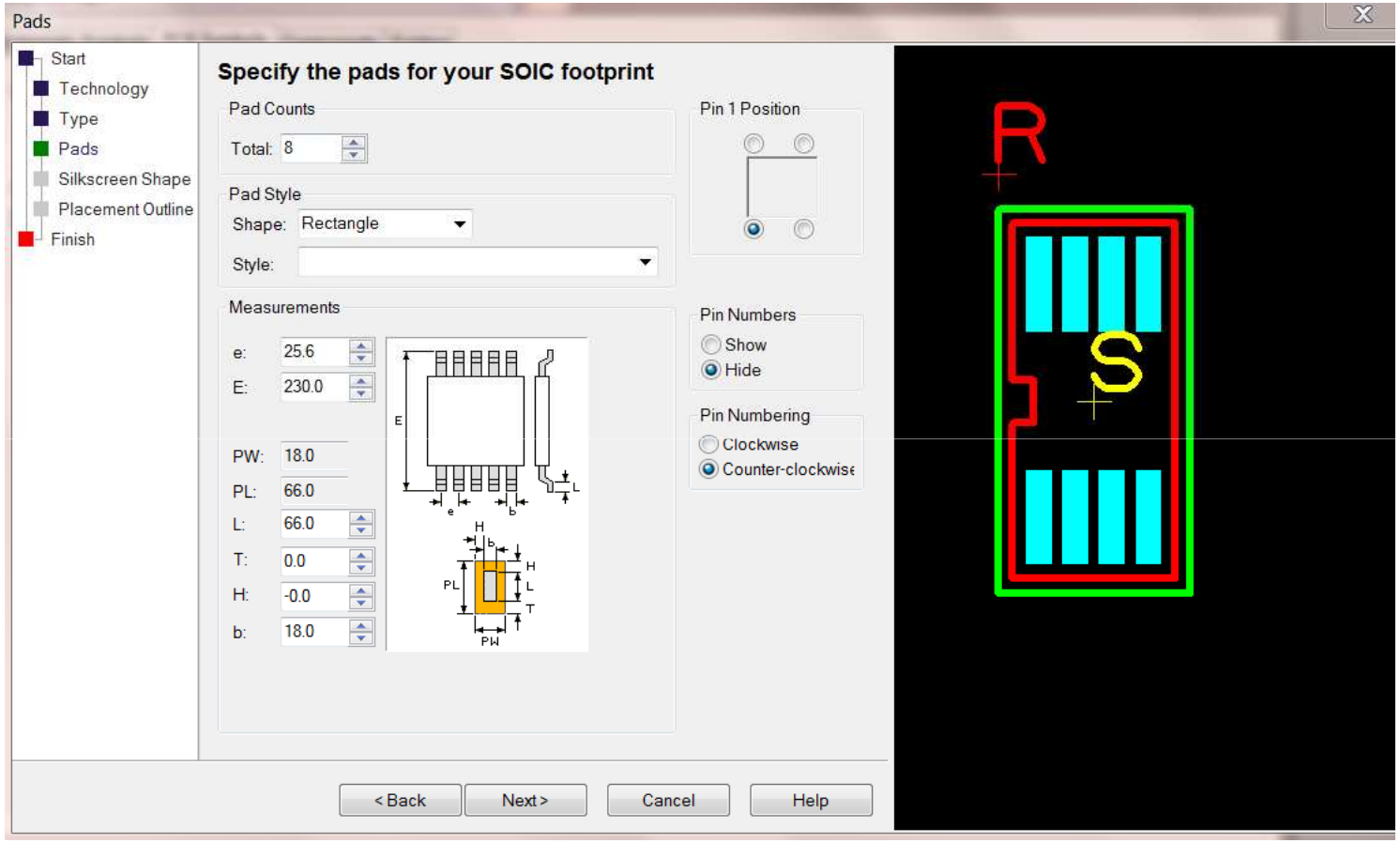
SOT-23-5	331	0.147	0.151	0.034	0.038	0.017	0.021	0.058	0.093	0.075	0.0374
SOT-23-6	332	0.147	0.151	0.034	0.038	0.017	0.021	0.058	0.093	0.075	0.0374
SOT-23-8	348	0.147	0.151	0.015	0.019	0.016	0.020	0.068	0.083	0.077	0.0256
MSOP-8	337	0.226	0.230	0.097	0.101	0.014	0.018	0.066	0.164	0.077	0.0256

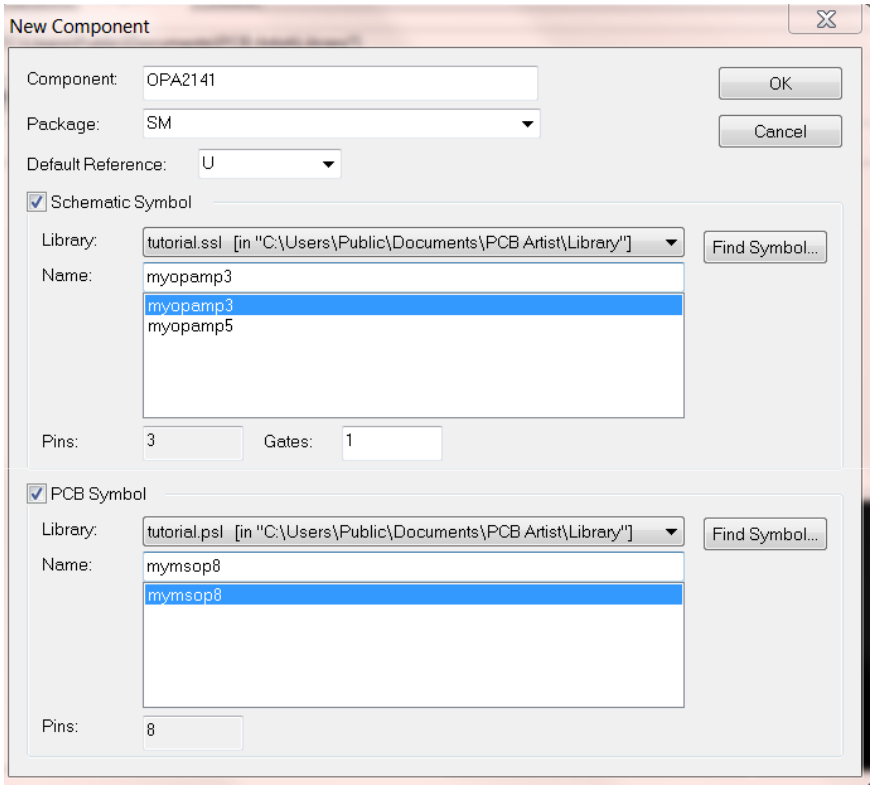
TABLE IV. Pad Dimensions—Inches.

New PCB Symbol



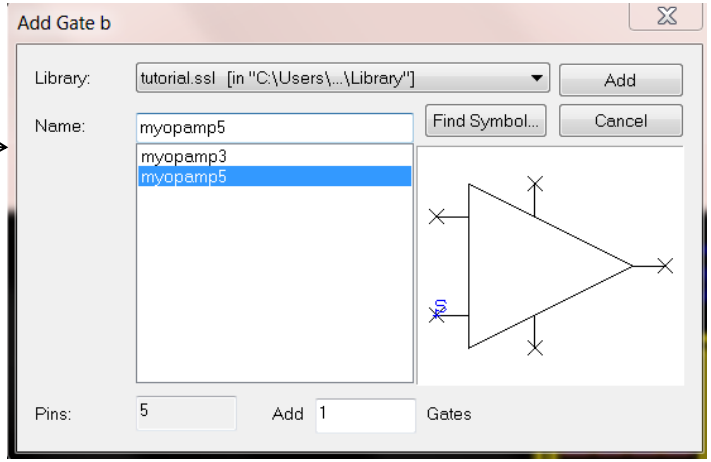
New Component

- Now we have the schematic and PCB symbols, we can combine them to create a component
- Create a new component library (make sure component tab is selected)
- Click New Item
- Only select one of the schematic symbols, we will add the other one later



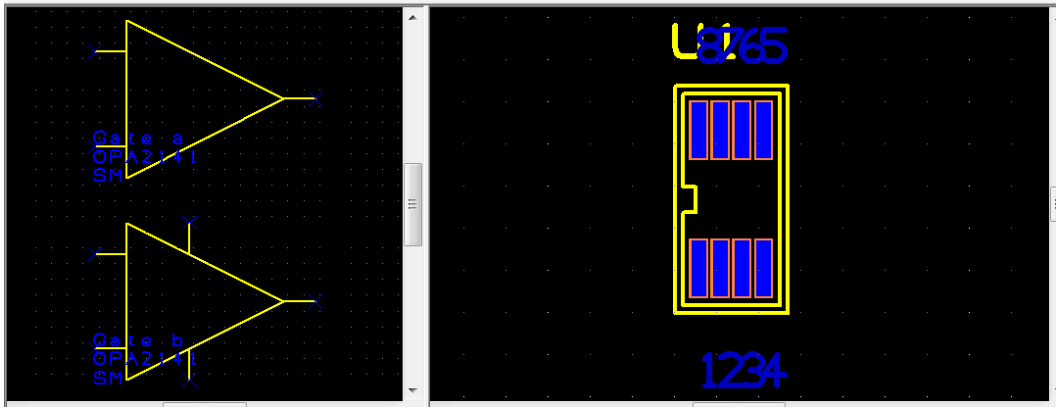
New Component

- Click Add Gate icon 
- Add 5-pin schematic symbol
- ‘a’ will zoom to all in schematic and PCB windows



Gate Name	Sch Symbol Name	Sch Symbol Terminal Nam	Sch Terminal Number	Pcb Symbol Pad Number	omponent Pin lame/Number	Net (Class) Name
a	myopamp3		1			
			2			
			3			
b	myopamp5		1			
			2			
			3			
			4			
			5			

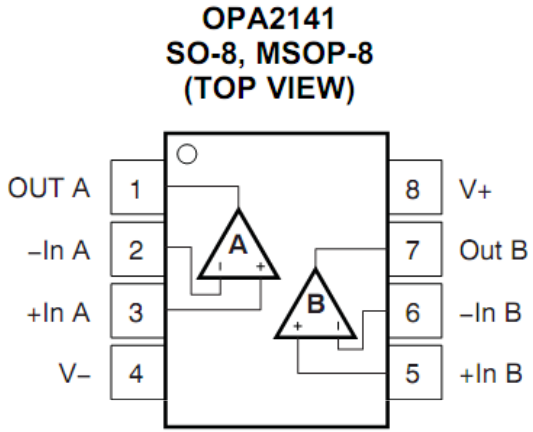
- You may have to right-click in top window to see spreadsheet

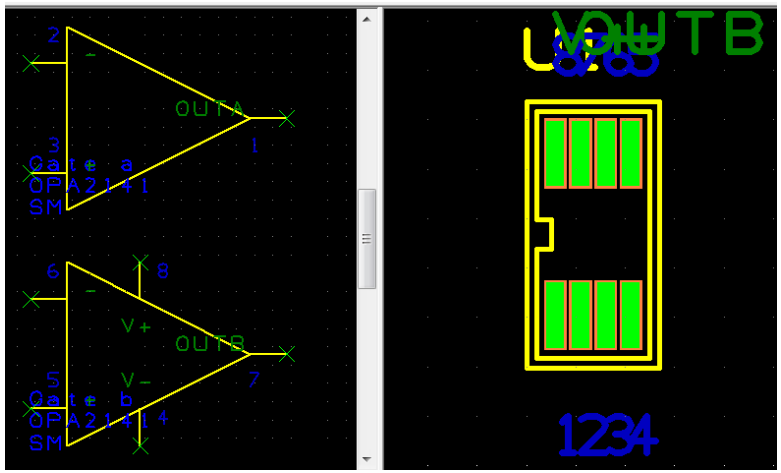


New Component

- Fill out spreadsheet according to datasheet block diagram & save component

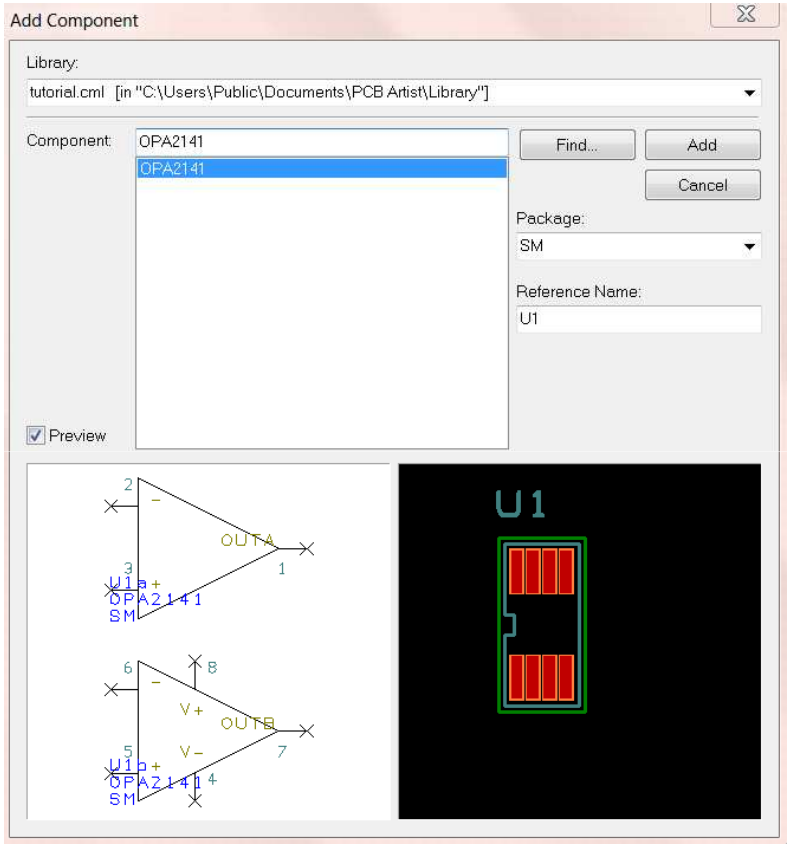
Gate	Sch Symbol	Sch Symbol	Sch Terminal	Pcb Symbol	Component Pin	Net (Class)
Name	Name	Terminal Nam	Number	Pad Number	Name/Number	Name
a	myopamp3	-	1	2	2	
		+	2	3	3	
		OUTA	3	1	1	
b	myopamp5	-	1	6	6	
		+	2	5	5	
		OUTB	3	7	7	
		V+	4	8	8	
		V-	5	4	4	

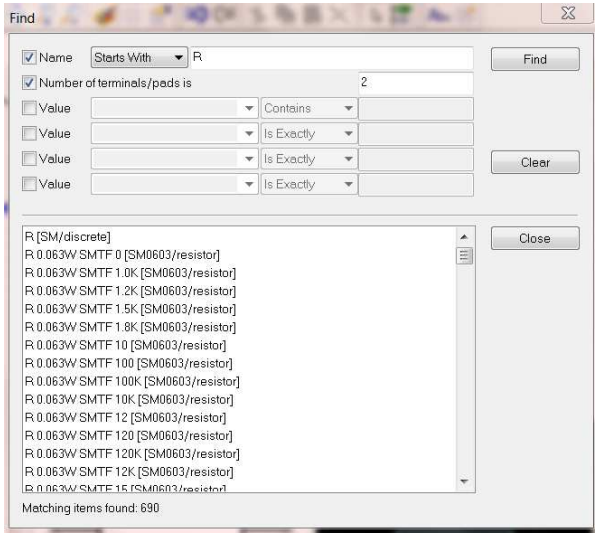




Create Schematic

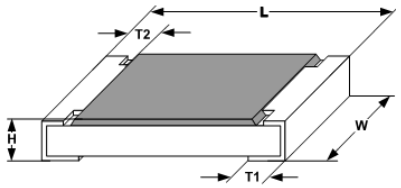
- Create Schematic in project
- Use Add Component to instantiate OPA2141 
- Note you can place each symbol separately
- Add Component->Find is very useful
  - R's are in library 'resistor'
  - C's are in library 'capacitor'

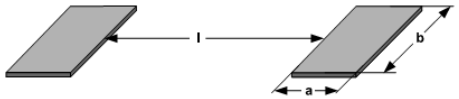




Create Schematic

- Common passive sizes are 0402, 0603, 0805, and 1206
- Probably want size 0805 at least for hand soldering



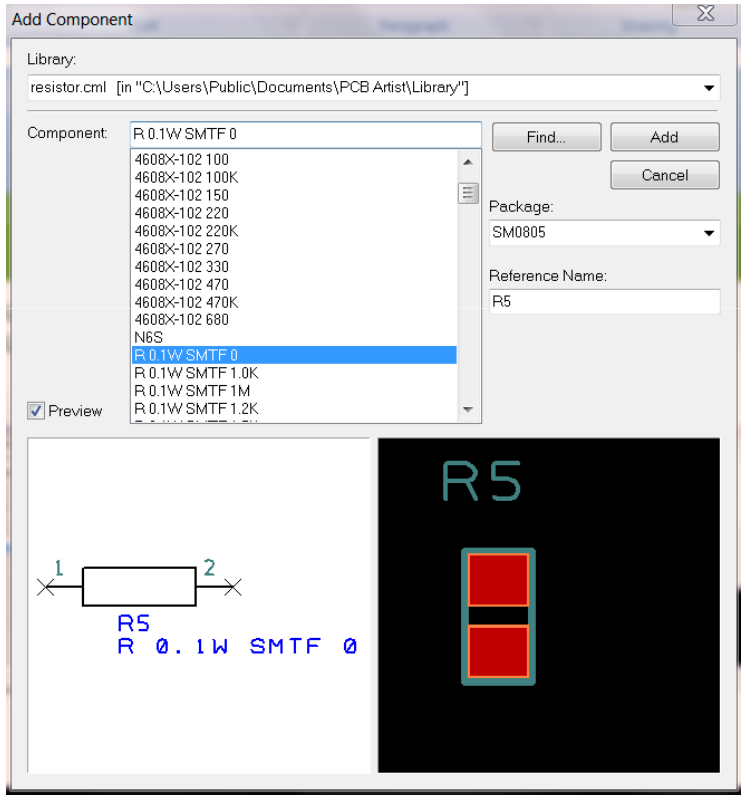


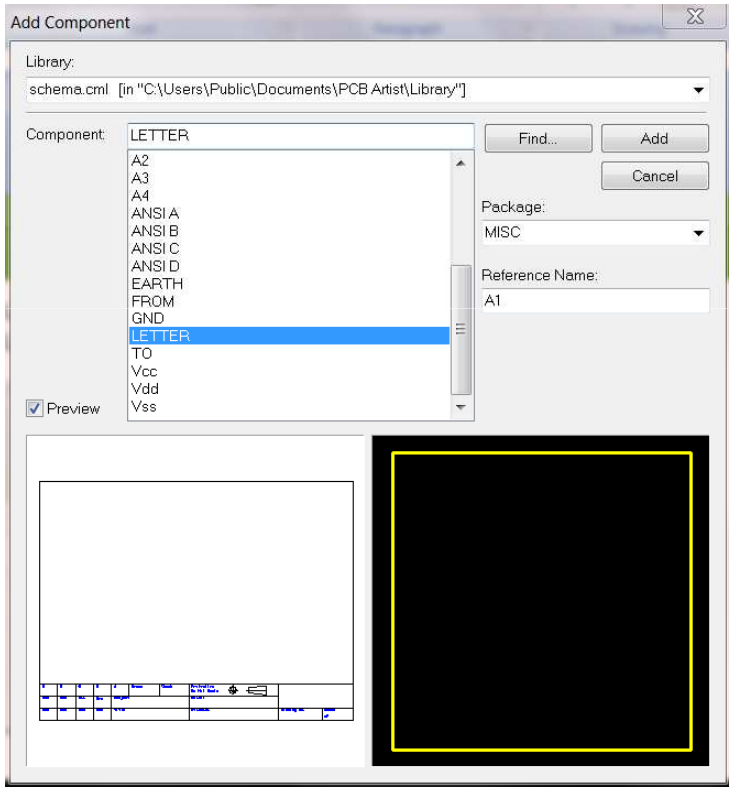
SIZE		DIMENSIONS in millimeters					SOLDER PAD DIMENSIONS in millimeters					
							REFLOW SOLDERING			WAVE SOLDERING		
INCH	METRIC	L	W	H	T1	T2	a	b	l	a	b	l
0402	1005	1.0 ± 0.05	0.5 ± 0.05	0.35 ± 0.05	0.25 ± 0.05	0.2 ± 0.1	0.4	0.6	0.5			
0603	1608	$1.55^{+0.10}_{-0.05}$	0.85 ± 0.1	0.45 ± 0.05	0.3 ± 0.2	0.3 ± 0.2	0.5	0.9	1.0	0.9	0.9	1.0
0805	2012	$2.0^{+0.20}_{-0.10}$	1.25 ± 0.15	0.45 ± 0.05	$0.3^{+0.20}_{-0.10}$	0.3 ± 0.2	0.7	1.3	1.2	0.9	1.3	1.3
1206	3216	$3.2^{+0.10}_{-0.20}$	1.6 ± 0.15	0.55 ± 0.05	0.45 ± 0.2	0.4 ± 0.2	0.9	1.7	2.0	1.1	1.7	2.3
1210	3225	3.2 ± 0.2	2.5 ± 0.2	0.55 ± 0.05	0.45 ± 0.2	0.4 ± 0.2	0.9	2.5	2.0	1.1	2.5	2.2
1218	3246	$3.2^{+0.10}_{-0.20}$	4.6 ± 0.15	0.55 ± 0.05	0.45 ± 0.2	0.4 ± 0.2	1.05	4.9	1.9	1.25	4.8	1.9
2010	5025	5.0 ± 0.15	2.5 ± 0.15	0.6 ± 0.1	0.6 ± 0.2	0.6 ± 0.2	1.0	2.5	3.9	1.2	2.5	3.9
2512	6332	6.3 ± 0.2	3.15 ± 0.15	0.6 ± 0.1	0.6 ± 0.2	0.6 ± 0.2	1.0	3.2	5.2	1.2	3.2	5.2

Note: 0.1mm~=4mils

Create Schematic

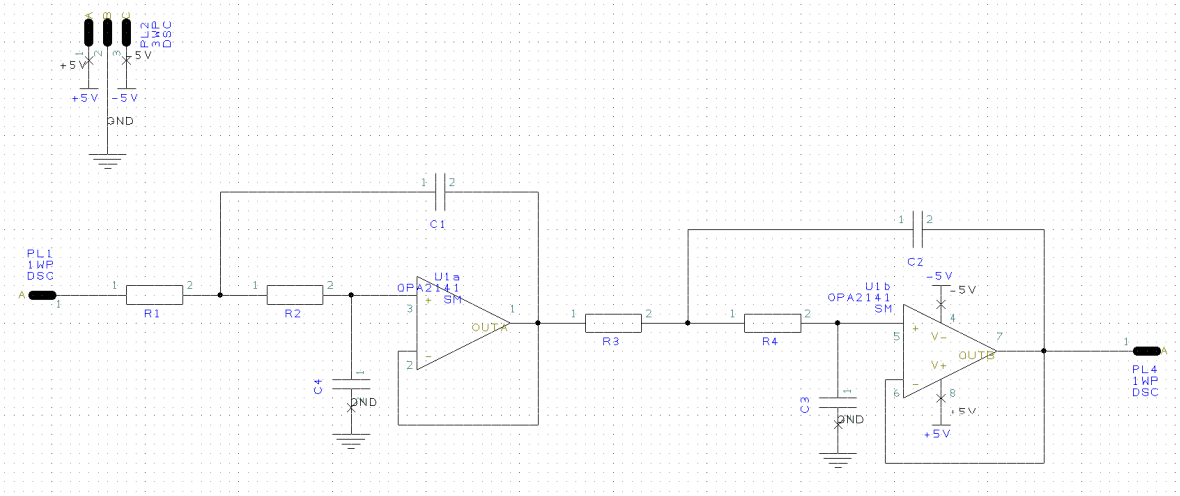
- Use ‘schema’ library for border (e.g. Letter) and power/ground
- Use ‘resistor’ and ‘capacitor’ libraries for R’s and C’s

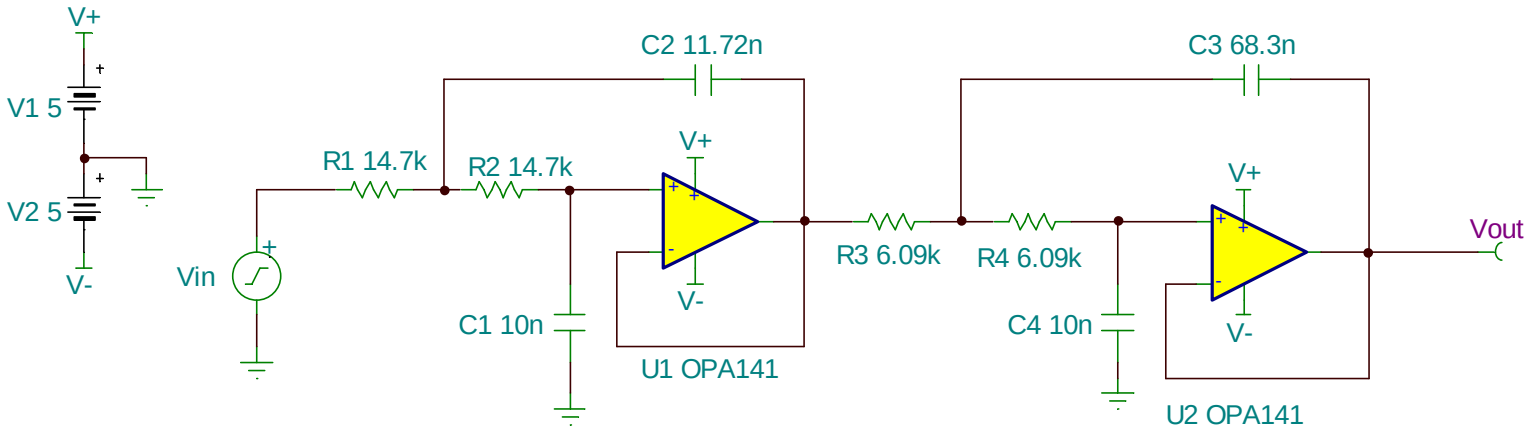




Create Schematic

- Use ‘connector’ library to add connectors or make your own





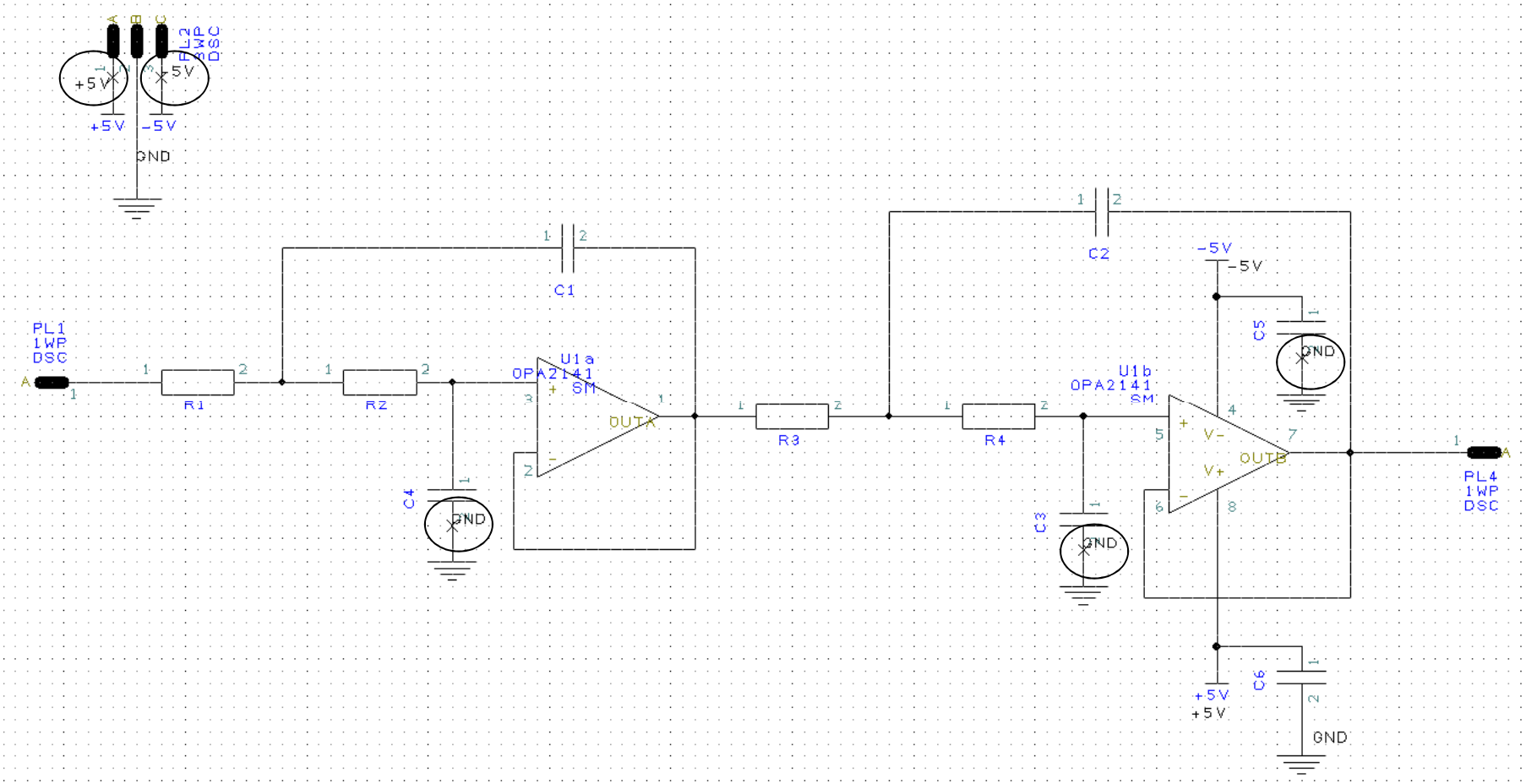
Create Schematic

- Are we missing anything?
- Check datasheets for layout recommendations
- From the OPA141 PDS:

> The OPA141, OPA2141, and OPA4141 are unity-gain stable, operational amplifiers with very low noise, input bias current, and input offset voltage. Applications with noisy or high-impedance power supplies require decoupling capacitors placed close to the device pins. In most cases, 0.1μF capacitors are adequate. Figure 1 shows a simplified schematic of the OPA141.

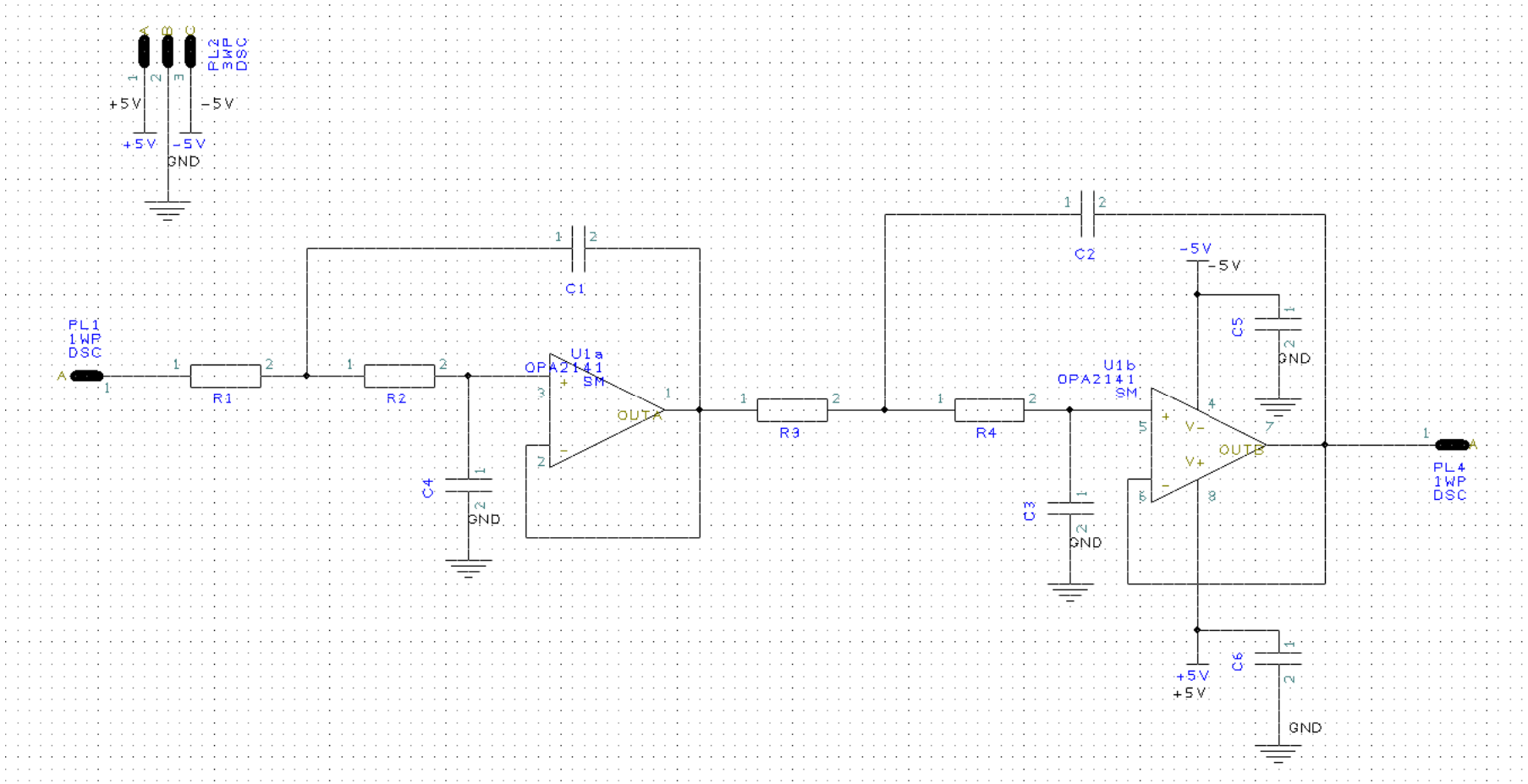
- So we need to add decoupling capacitors near the device's supply

Create Schematic



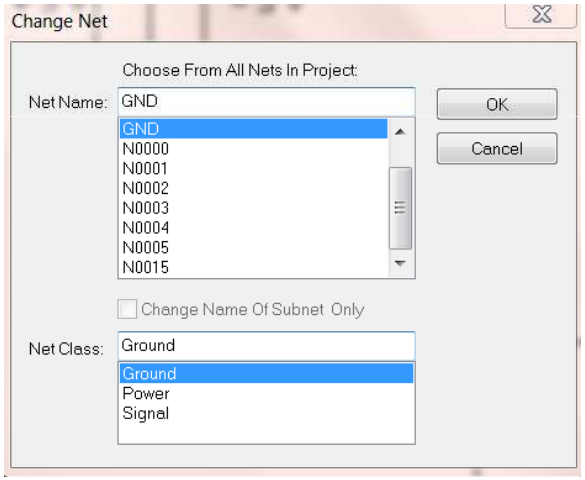
These are bad! Must use wire to connect!

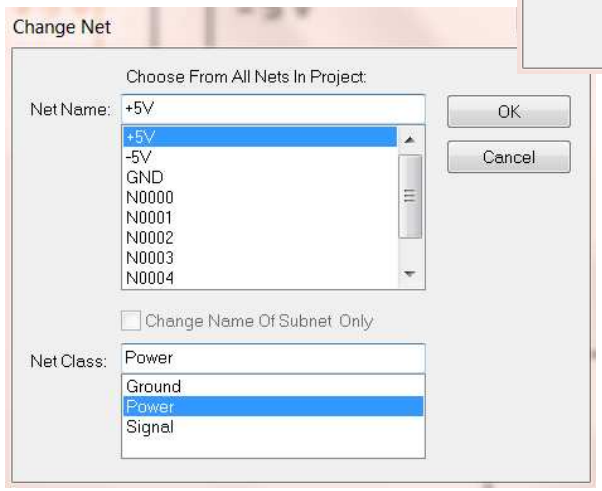
Create Schematic

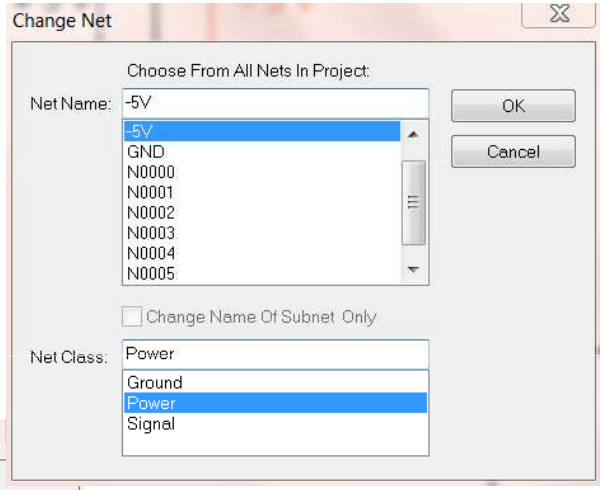


Create Schematic

- Finally, we need to ensure that our power and ground nets are set appropriately
  - Right-click a ground symbol
  - Select “Change Net”
  - Make sure net name and net class are set appropriately
  - Also do this for +5V and -5V

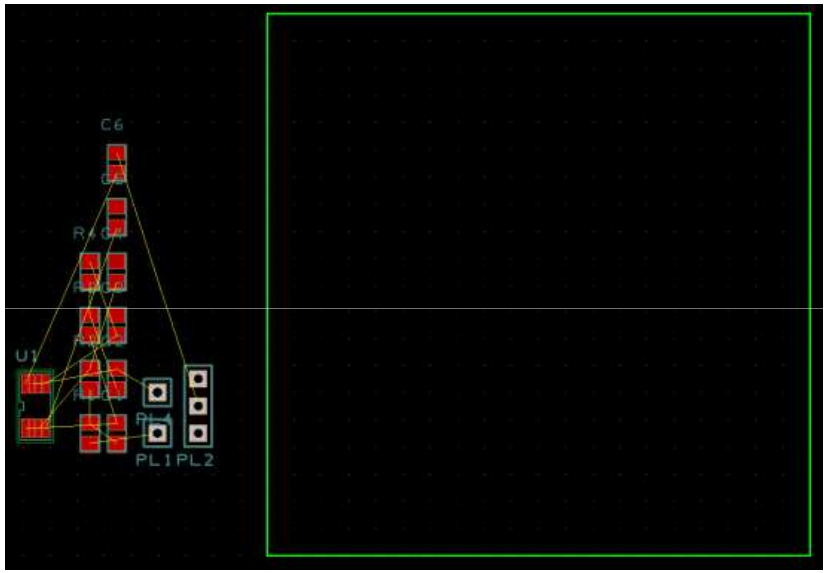






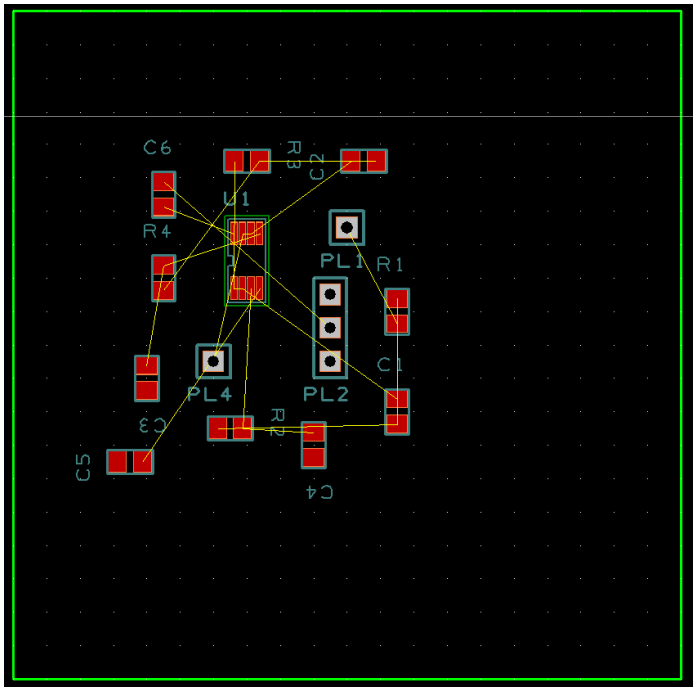
Create PCB

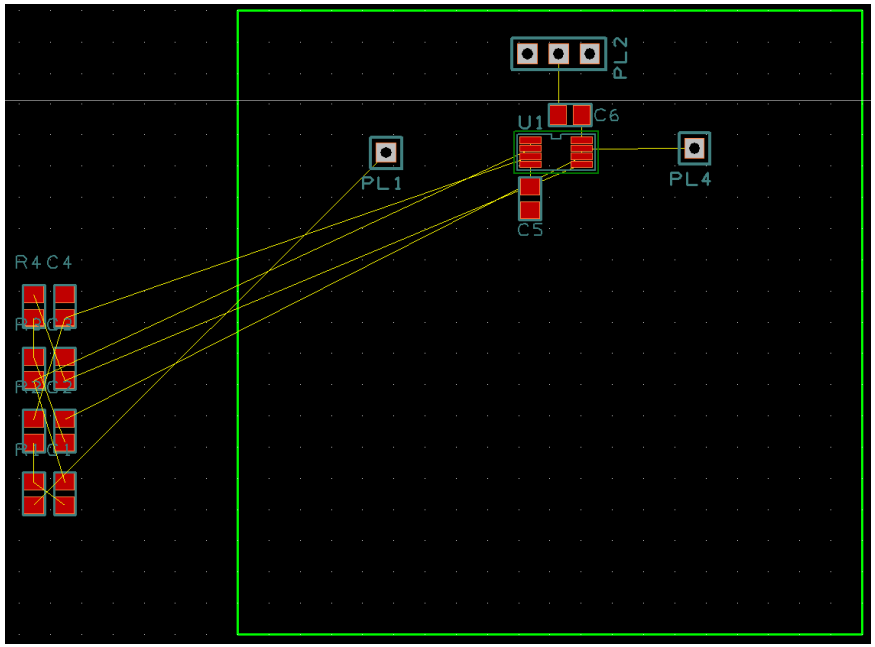
- Save and close schematic
- Open Layout
- Import footprints from Schematic
  - Tools->[Schematic<->PCB]->Consistency Check
    - I recommend performing Consistency Checks frequently during a design
  - Yes
  - OK
  - ‘a’ to zoom all
  - Select all footprints and move them outside PCB border
  - ‘a’ to zoom all



Create PCB

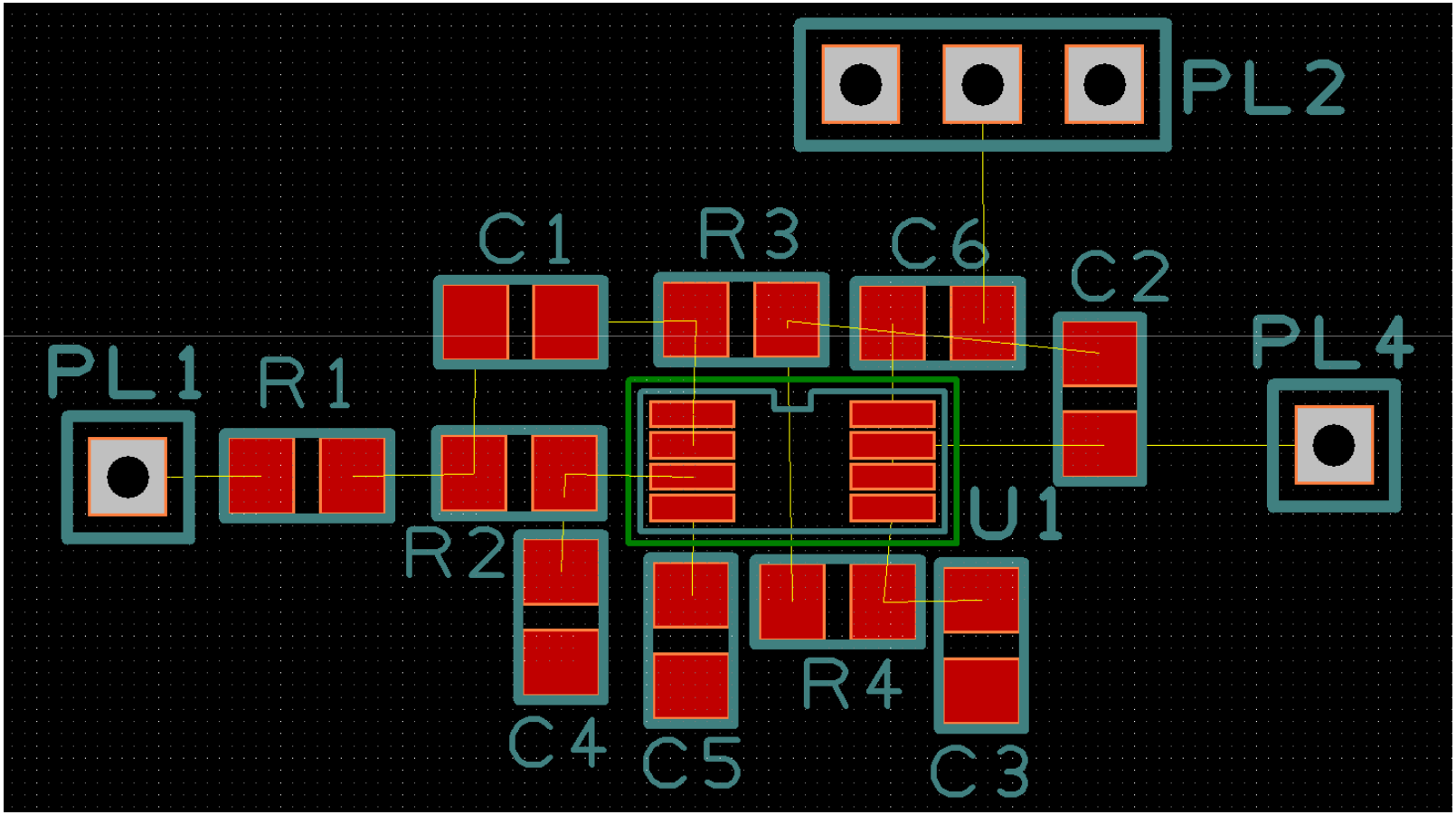
- Yellow lines are connections that need to be made
  - Sometimes called ‘rubber bands’
- Place components inside green PCB border
  - PCB Artist has an ‘autoplace components’ feature, but it doesn’t seem to work well
  - Place the OPA2141, power connector, input connector, output connector, and decoupling caps
  - In general, place inputs on left side of board, outputs on right, and power at top or bottom





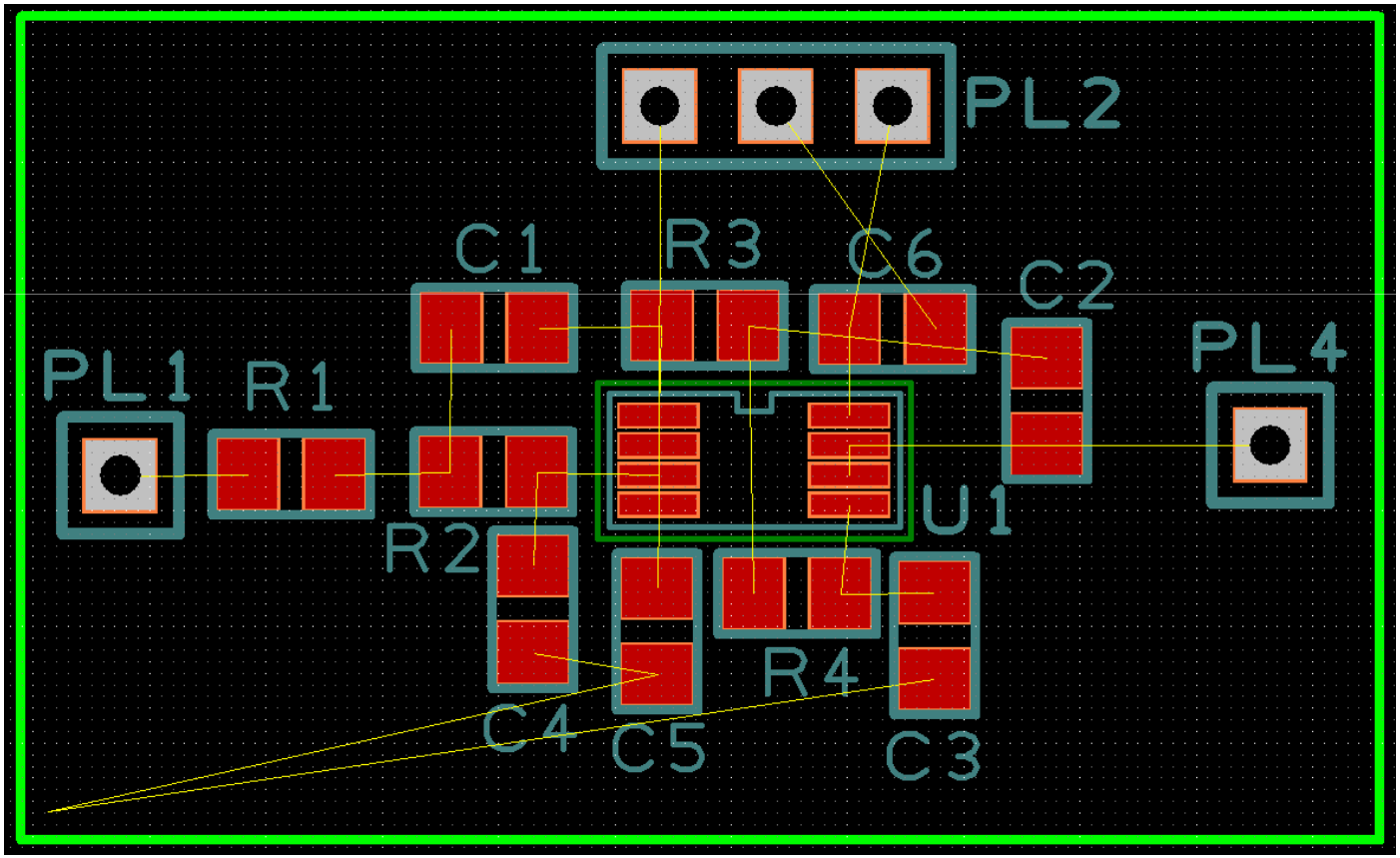
Create PCB

Notice lack of bands for supplies? This is because they weren't connected in schematic! (Remember the 'X's?)



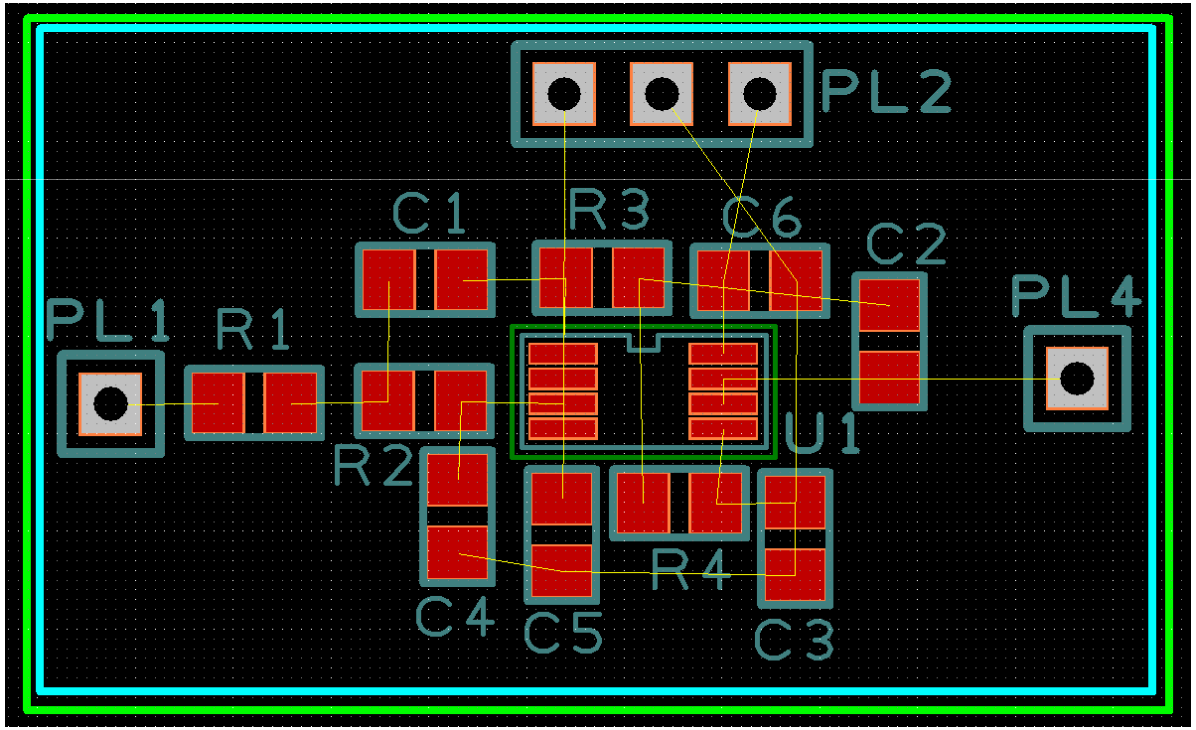
Create PCB

Supply nets and grounds are now connected. Also fit board outline. *Run DRC often!* Tools->DRC (check Spacing and Manufacturing)



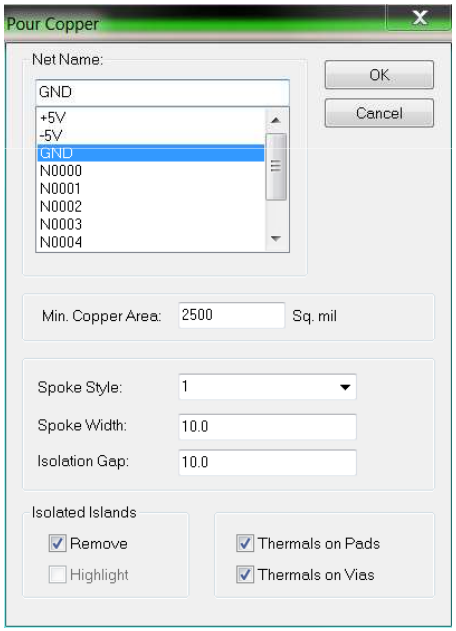
Create PCB

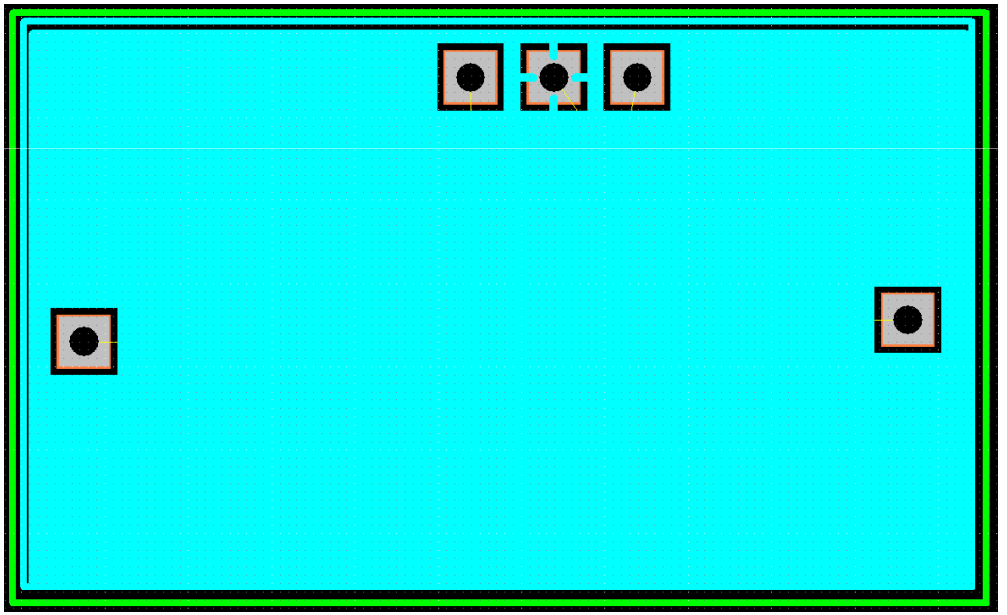
- Since we have 2 layers, let's make the bottom layer GND
- Need to perform a 'pour'
  - Add->Copper Pour->Rectangle
  - Press "L" to change layer to 'bottom'
  - Create rectangle inside board outline

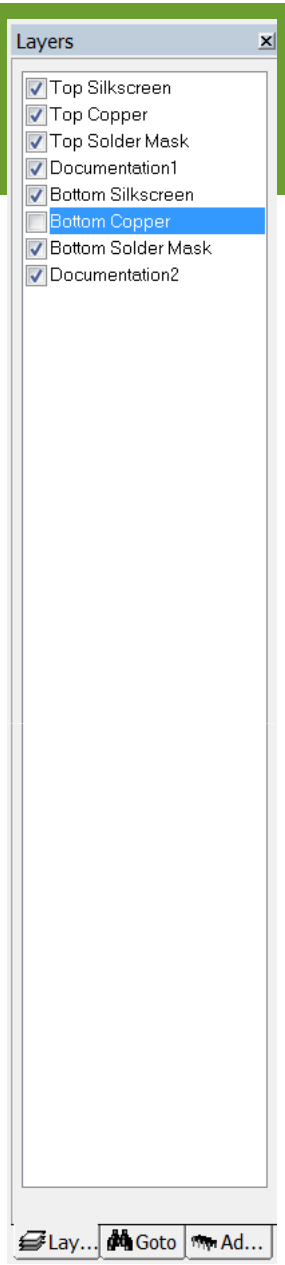


Create PCB

- Right click copper pour outline and select ‘Pour Copper’
- Assign to GND net and click OK
- To hide bottom layer, press F9, select Layers tab, and uncheck ‘Bottom Copper’
- Now we can use vias to connect to GND

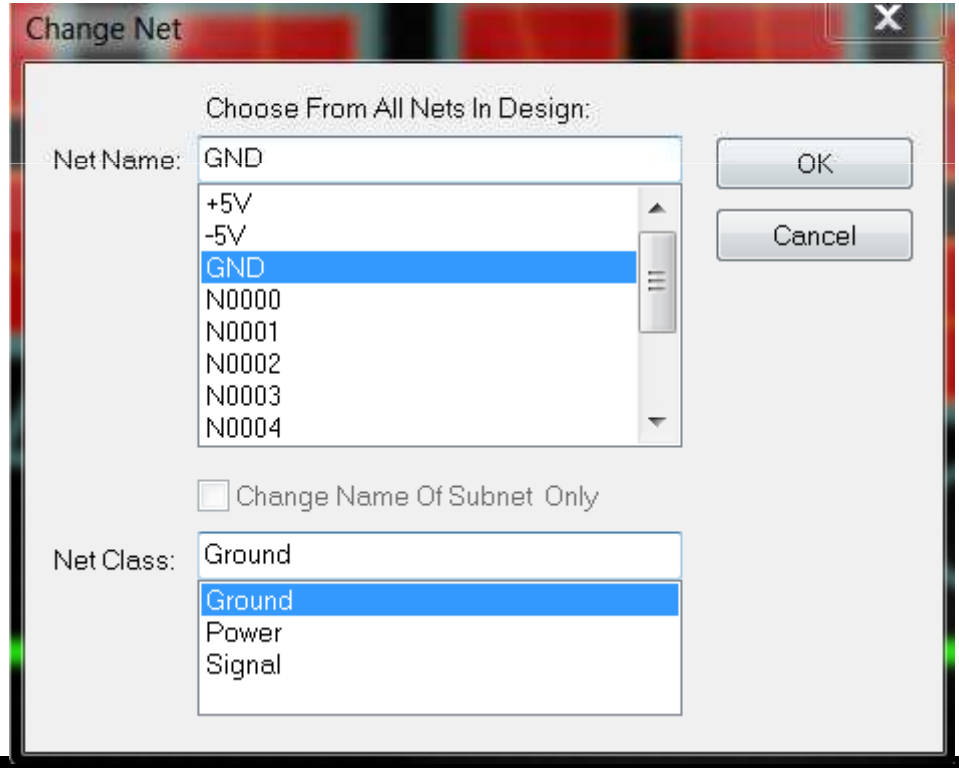






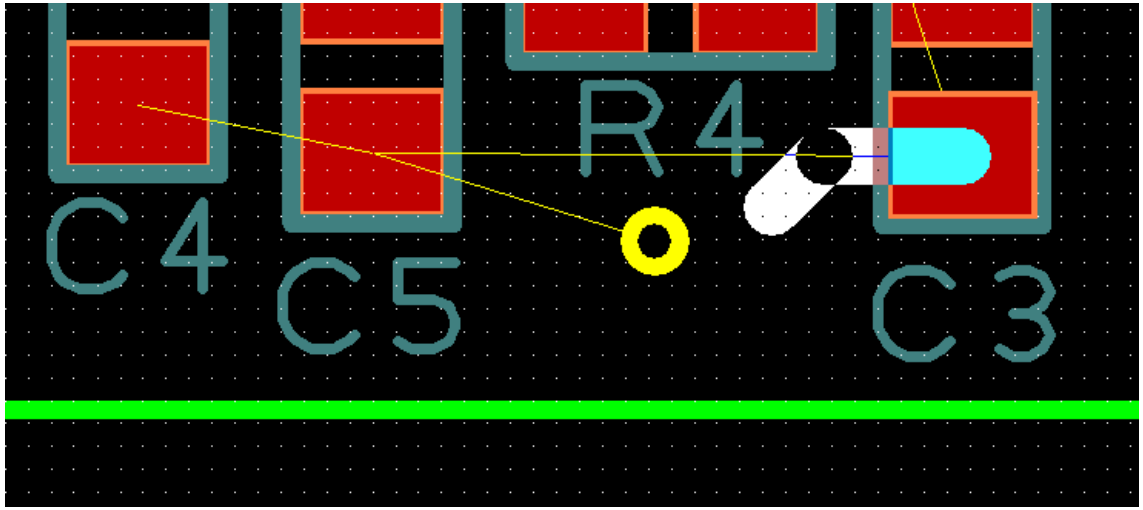
Create PCB

- We know C3, C4, and C5 are all grounded
- We can place a via to connect them to the ground plane
  - Add->Via
  - ‘Esc’ stops placement
- Once placed, right-click via and add to GND net (Net->Change Net)



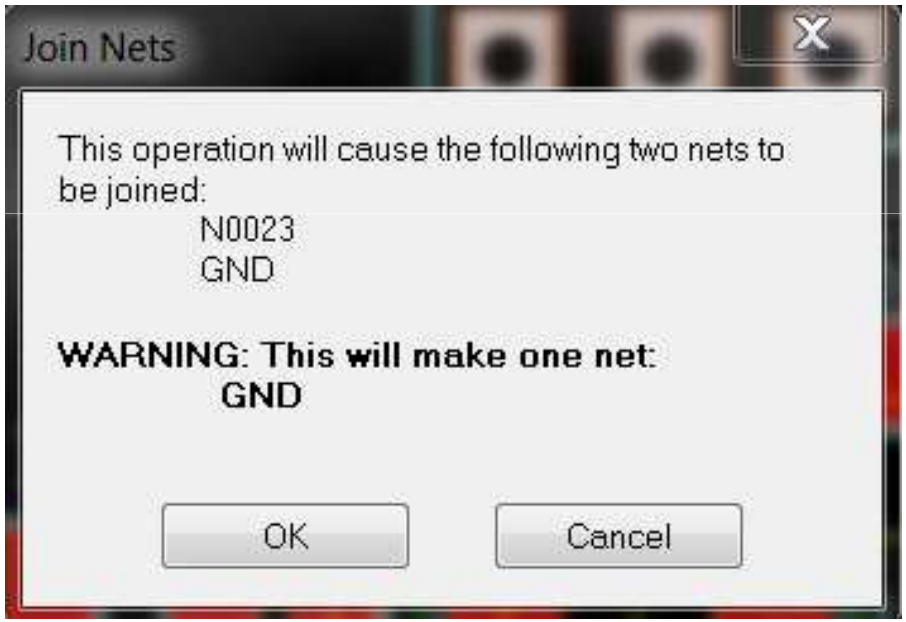
Create PCB

- To route a trace to the via, double-click the pad of the footprint (notice the trace is 25mils wide)
- Drag trace to via and double-click again
- Do this for all GND nets
- Bands didn't disappear, press 'ctrl-d' to 'optimize nets' (in tools menu)
- You can left-click band and press delete
- If bands are missing, try performing a 'consistency check' from tools menu



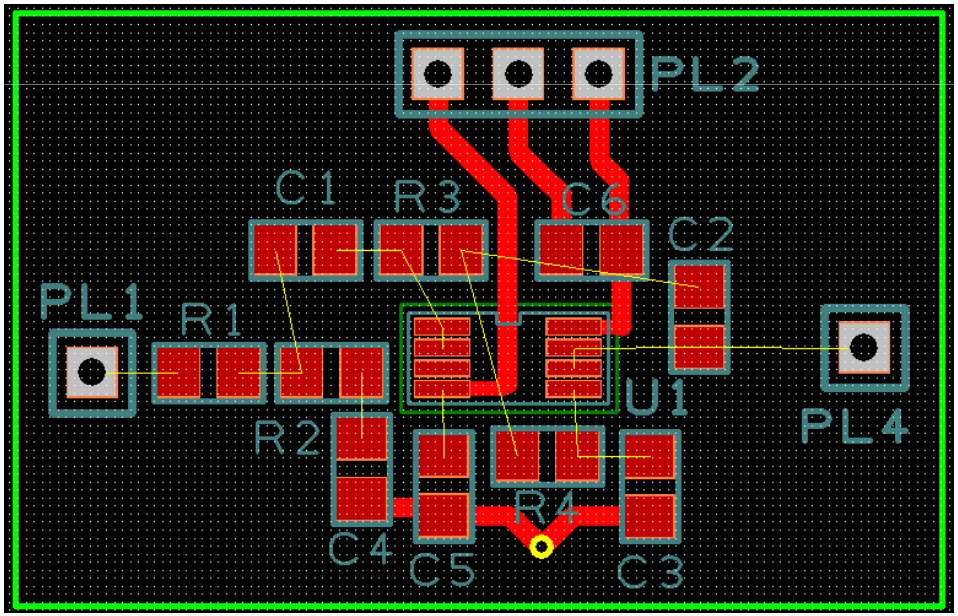
Create PCB

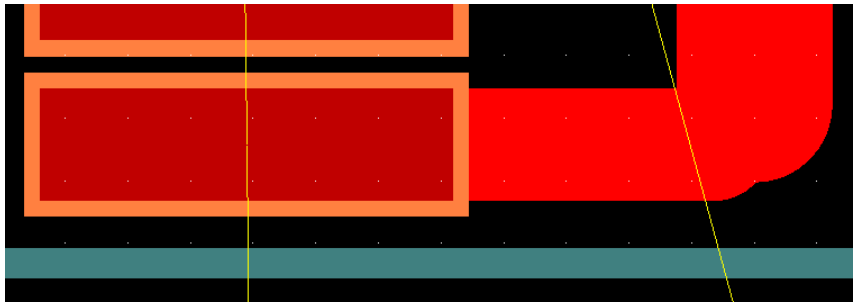
- You may get a join nets box
- The order depends on where you start and end your trace
- To switch the order, route in the reverse order



Create PCB

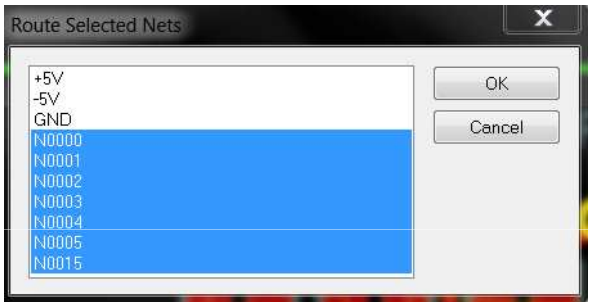
- I would hand-route power and GND first.
- Since power traces are wider than MSOP-8 pads, route as close to pad as possible with thick trace. Then route from pad to thick trace. While routing from pad to thick trace, press S and change width to 18
- Run DRC often! Don’t forget Ctrl-D and Consistency Checks!





Create PCB

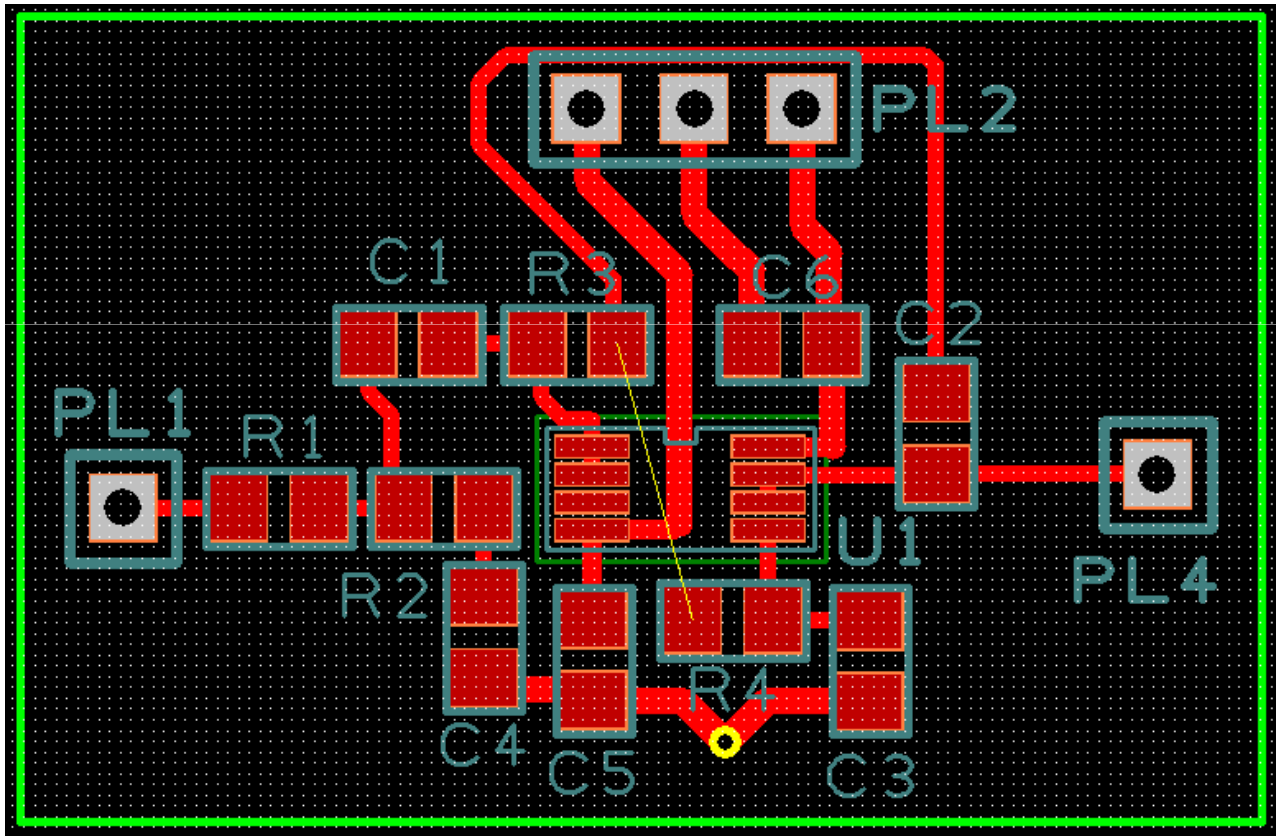
- You can try autorouting (3 methods)
  - Right click a band and select ‘autoroute’ to route 1 trace at a time
  - Tools->Autoroute Nets->All Nets to route all nets (it will remove your existing routes)
  - Tools->Autoroute Nets->Browse Nets (we will do this since we already routed power and GND)



- This didn’t work well for me, and I prefer to do it by hand anyways

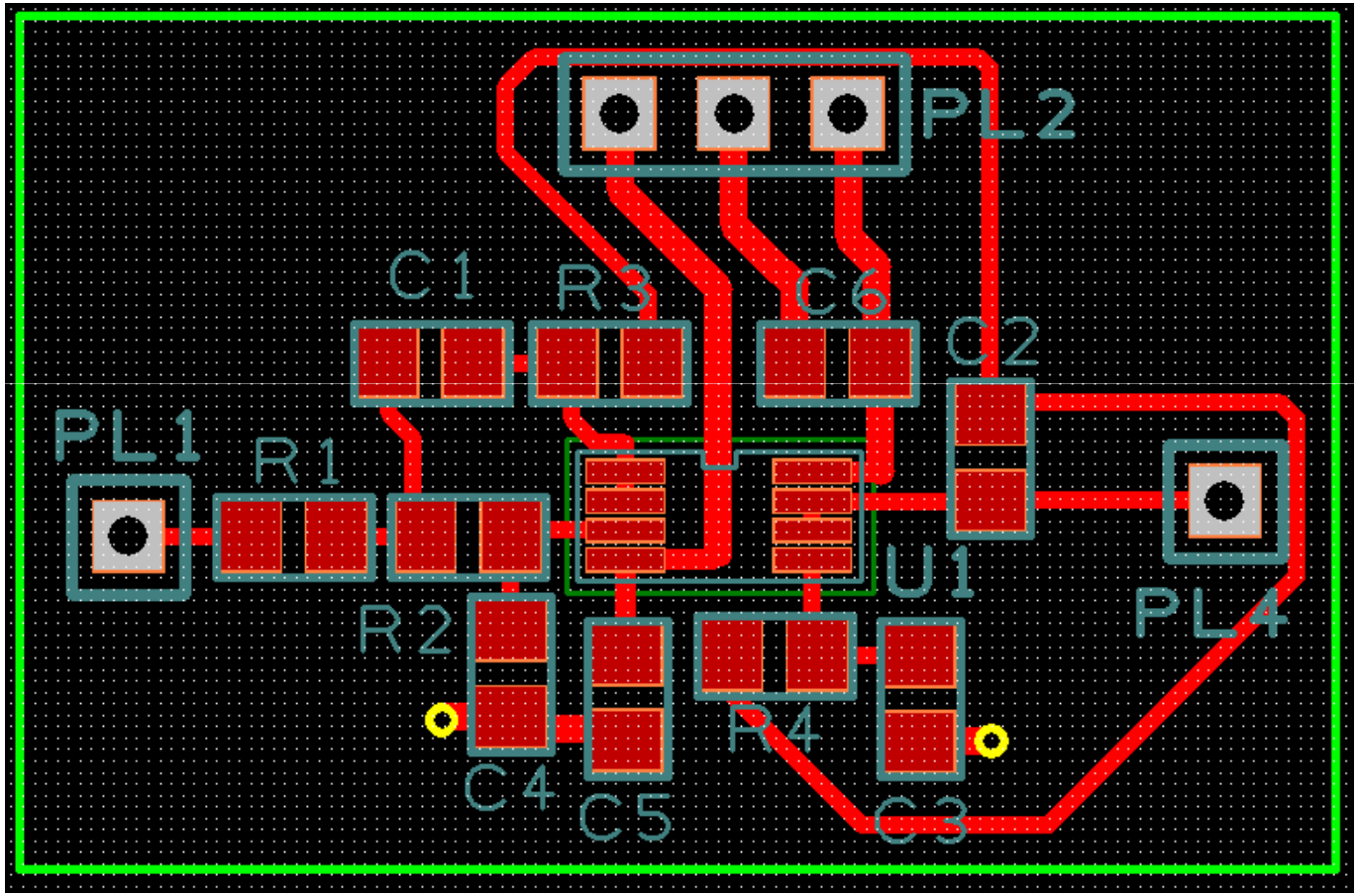
Create PCB

- Almost done
- Are we stuck??



Create PCB

- Nope!



Create PCB-Reflection

- Some of the traces were long
- We could have looked at using a 4-layer board
- We also didn’t have to devote an entire routing plane to ground
- We could also have separated V+, V-, and GND connectors and moved them to more convenient locations.

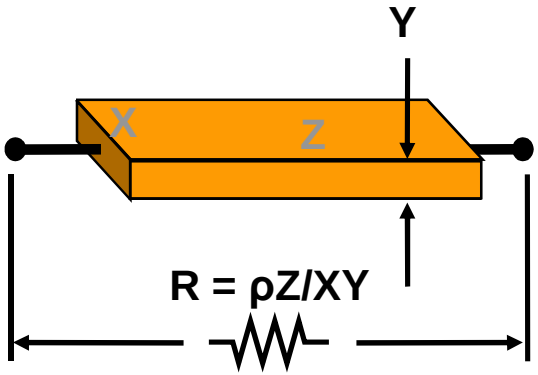
Fabricate PCB

- Be sure to run a DRC with all boxes checked
- Output->Submit Order
- Follow the directions
  - You will need to setup an AC account
- Alternately, I could submit the order for you.

PCB Layout Tips from TI

All Materials have a Finite Resistance

For PCB Trace



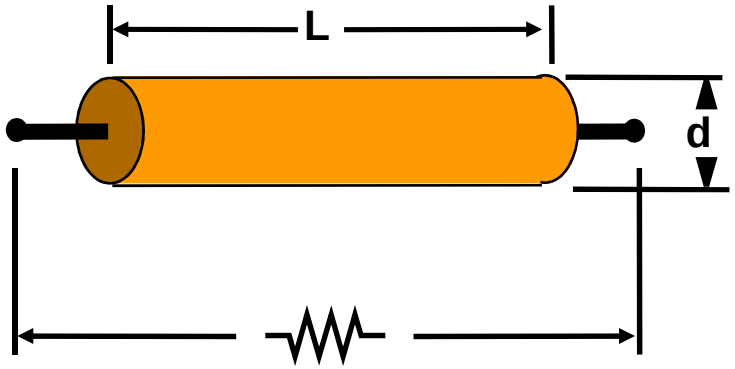
For 1 oz. Copper:

ρ = 1.724 x 10^{-6} ∧-cm for Y = 0.0038cm

R = 0.45 Z/X m∧ = number of "squares"

R = sheet resistance for 1 "square"
(Z = X) = 0.45m∧/square

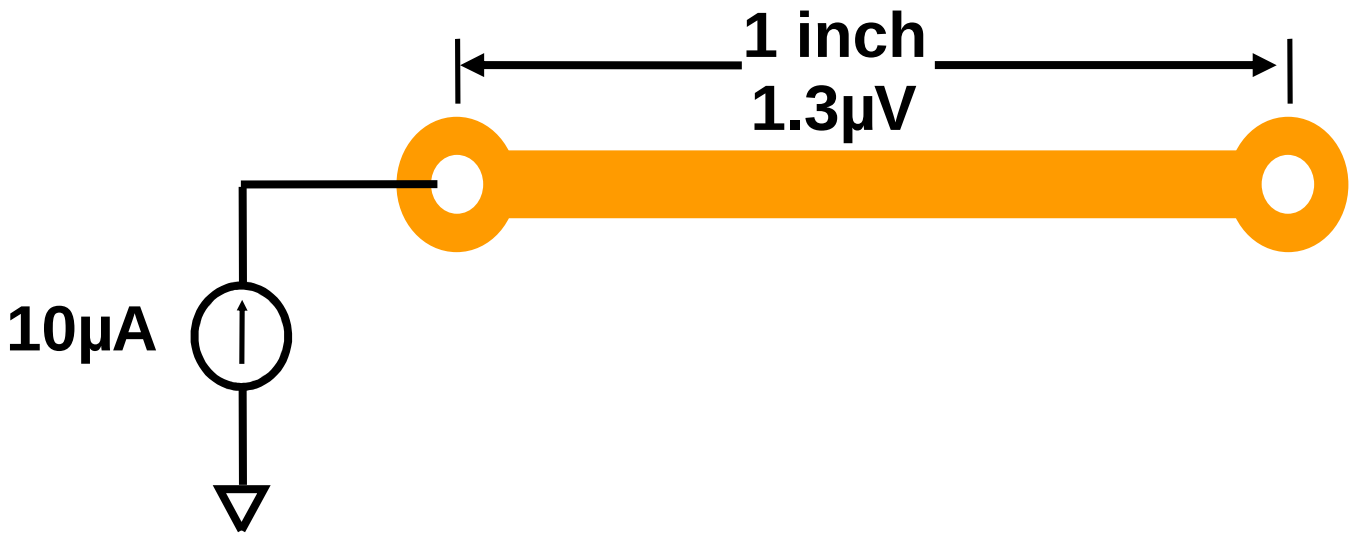
For Wire



$$R = \frac{0.0219L}{d^2}$$

L in meters
d in mm

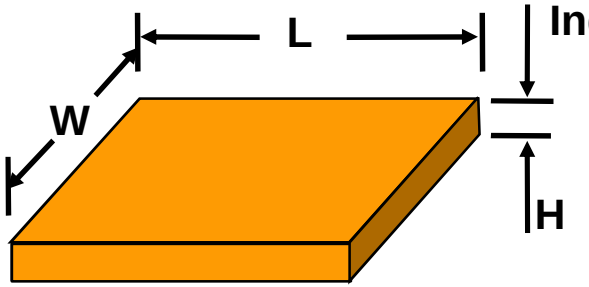
PCB Trace Resistance



- 1 inch (7 mil) trace of 1/2 oz copper with 10µA of current => voltage drop of 1.3µV
- **4 LSBs (298nV) at 24 bits!**

PCB Inductance

PCB:



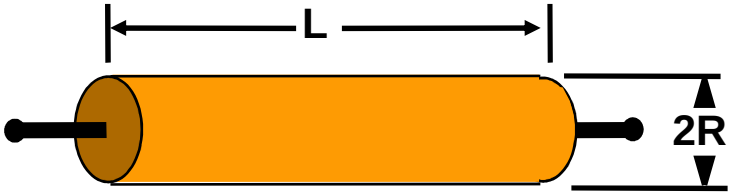
$$\text{Inductance} = 0.0002L\left[\ln\left(\frac{2L}{W+H}\right) + 0.2235\left(\frac{W+H}{L}\right) + 0.5\right] \text{ H}$$

Example:

L	= 10cm
W	= 0.25mm
H	= 0.038mm

This PC track has 141nH of inductance

Wire:



$$\text{Inductance} = 0.0002L\left[\ln\left(\frac{2L}{R}\right) - 0.75\right] \text{ H}$$

Example:

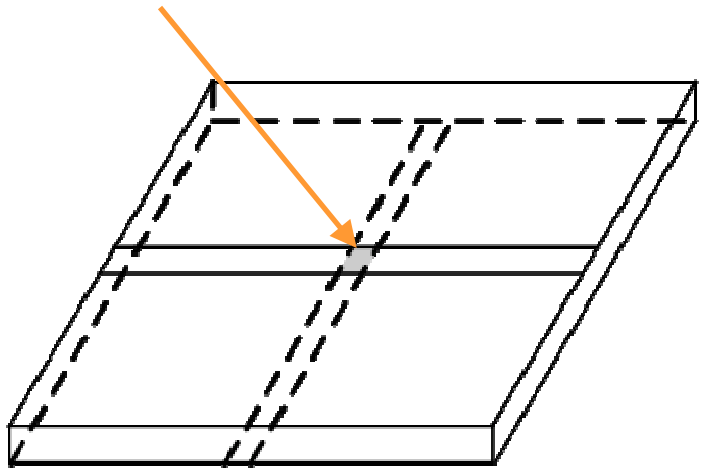
L	= 10cm
2R	= 0.5mm

This wire has 105nH of inductance

PCB Capacitance

- Two Cu plates with PCB material dielectric
  - Two 10 mil traces on a multi layer PCB, 10 mil between layers

A = 0.25 mm x 0.25 mm



Note: 10 mil = 0.25 mm.

$$C = \frac{\varepsilon_R \times \varepsilon_O \times A}{t}$$

Permittivity of FR4 ≈ 4.7

$\sum_o = 8.84 \times 10^{-12}$

$$C = \frac{\left(41.9 \times 10^{-12}\right) A}{t}$$

$$C = \frac{\left(41.9 \times 10^{-12}\right)\left(0.25 \times 10^{-3}\right)^2}{0.25 \times 10^{-3}}$$

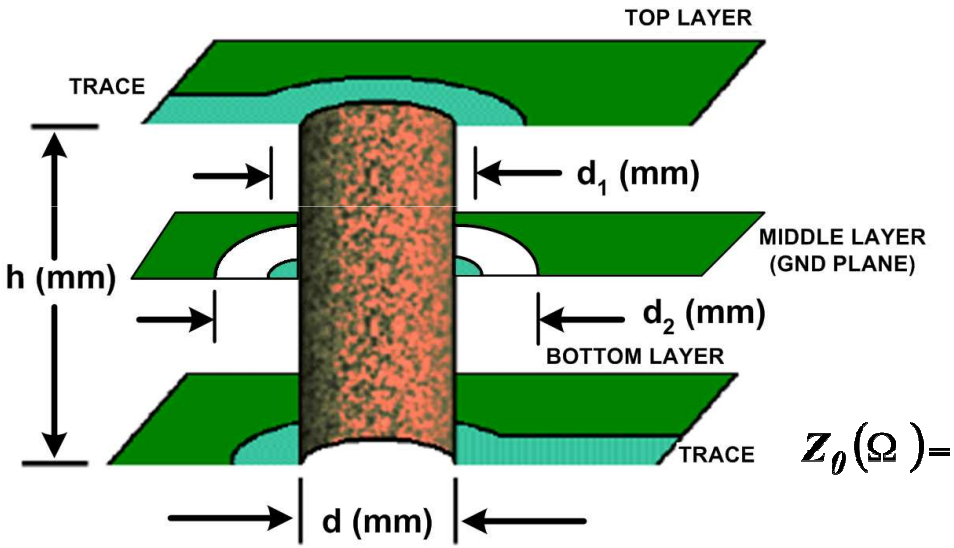
$$C = 0.01\ pF$$

PCB Vias

Component: Vias

Purpose: Interconnect traces on different layers

Problem: Inductance and Capacitance



$$L(nH) \approx \frac{h}{5}\left[1 + ln\left(\frac{4h}{d}\right)\right]$$

$$C(pF) \approx \frac{0.0555\,\varepsilon_r\, h\, d_1}{d_2 - d_1}$$

$$Z_0(\Omega) = 31.6\sqrt{\frac{L(nH)}{C(pF)}} \qquad T_p(ps/cm) = 31.6\sqrt{L(nH)C(pF)}$$

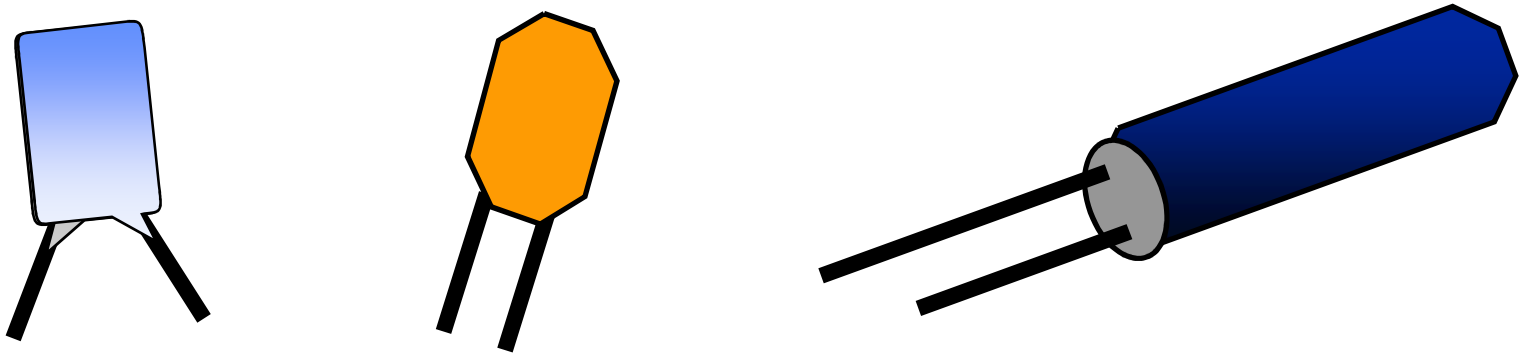
0.4mm (0.0157”) via with 1.6mm (0.063”) thick PCB has ≈ 1.2nH

1.6mm (0.063”) Clearance hole around 0.8mm (0.031”) pad on FR-4 has ≈ 0.4pF

e_r = PCB material permeability (FR-4 ≈ 4.5)

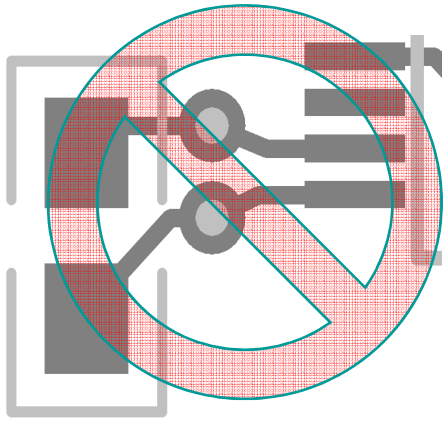
Bypass Capacitors

- Used in all analog applications
- Used for bypassing (cleaning up) power supplies
- Most op amp applications use two types for the two roles they must fill

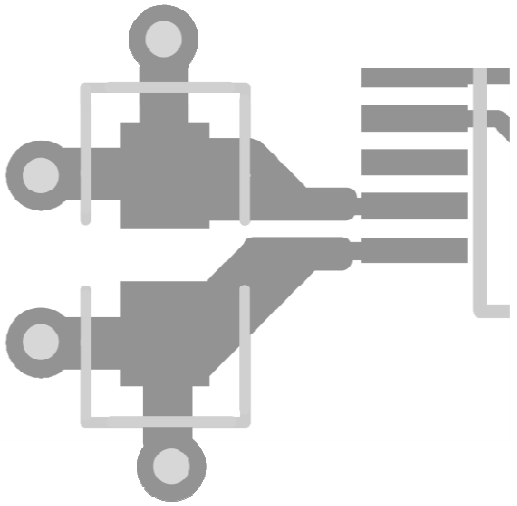


Bypass Capacitors

- DO NOT have vias between bypass caps and active device – Visualize the high frequency current flow !!!
- Ensure Bypass caps are on same layer as active component for best results.
- Route vias into the bypass caps and then into the active component.
- The more vias the better.
- The wider the traces the better.
- The closer the better



Poor Bypassing

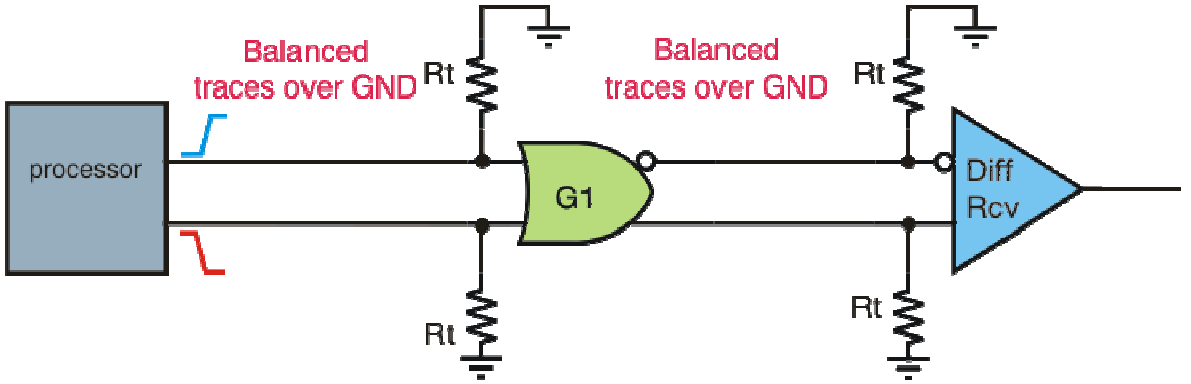


Good Bypassing

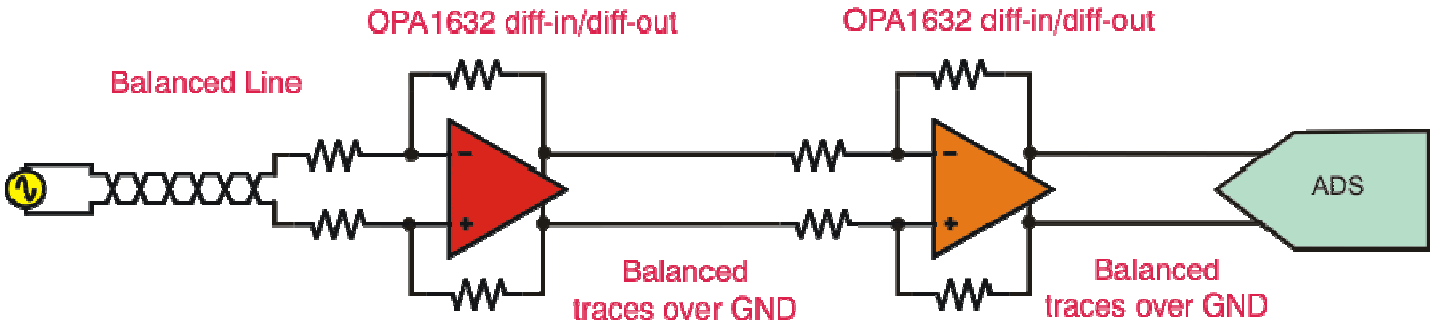
Balanced analog and digital circuit

(common-mode signals not welcome!)

Balanced digital logic: LVDS, PECL, HSTL



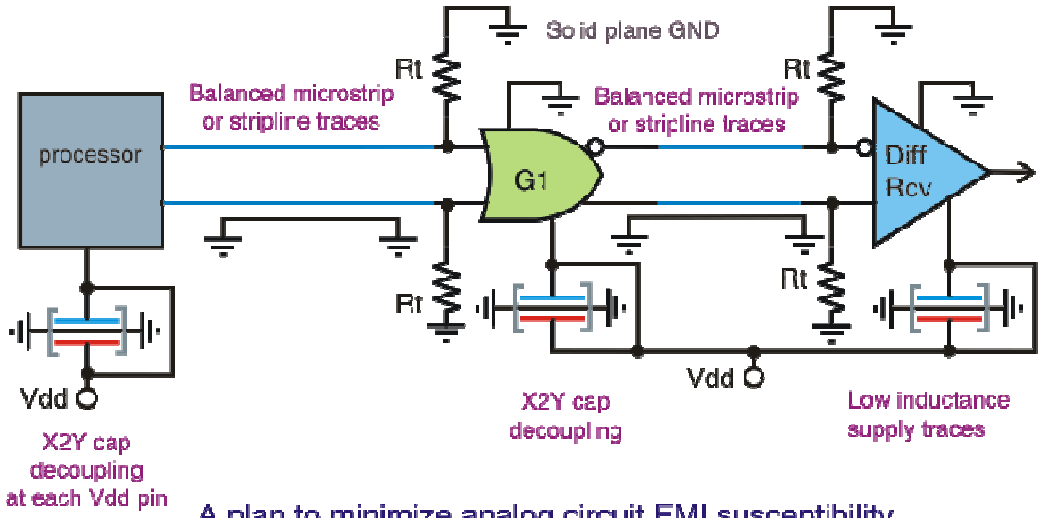
Balanced differential analog circuitry



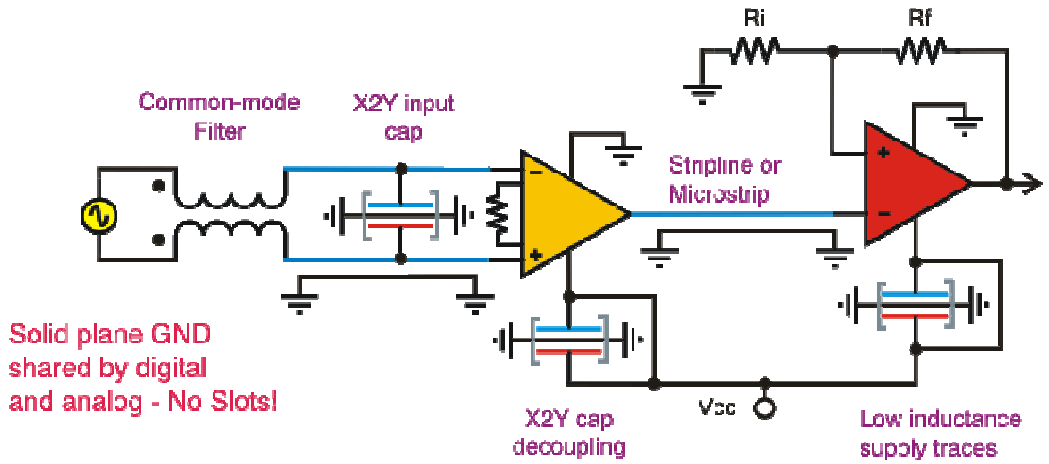
Circuit techniques to minimize EMI

- Strive for a zero impedance ground
- Design for a differential signal environment, both logic and analog
- Minimize PCB loops that act as EMI antennas
- Use X2Y capacitors for filtering and decoupling
- Make use of common-mode transformers
- Use balanced lines and traces

A plan to reduce digital circuit EMI generation



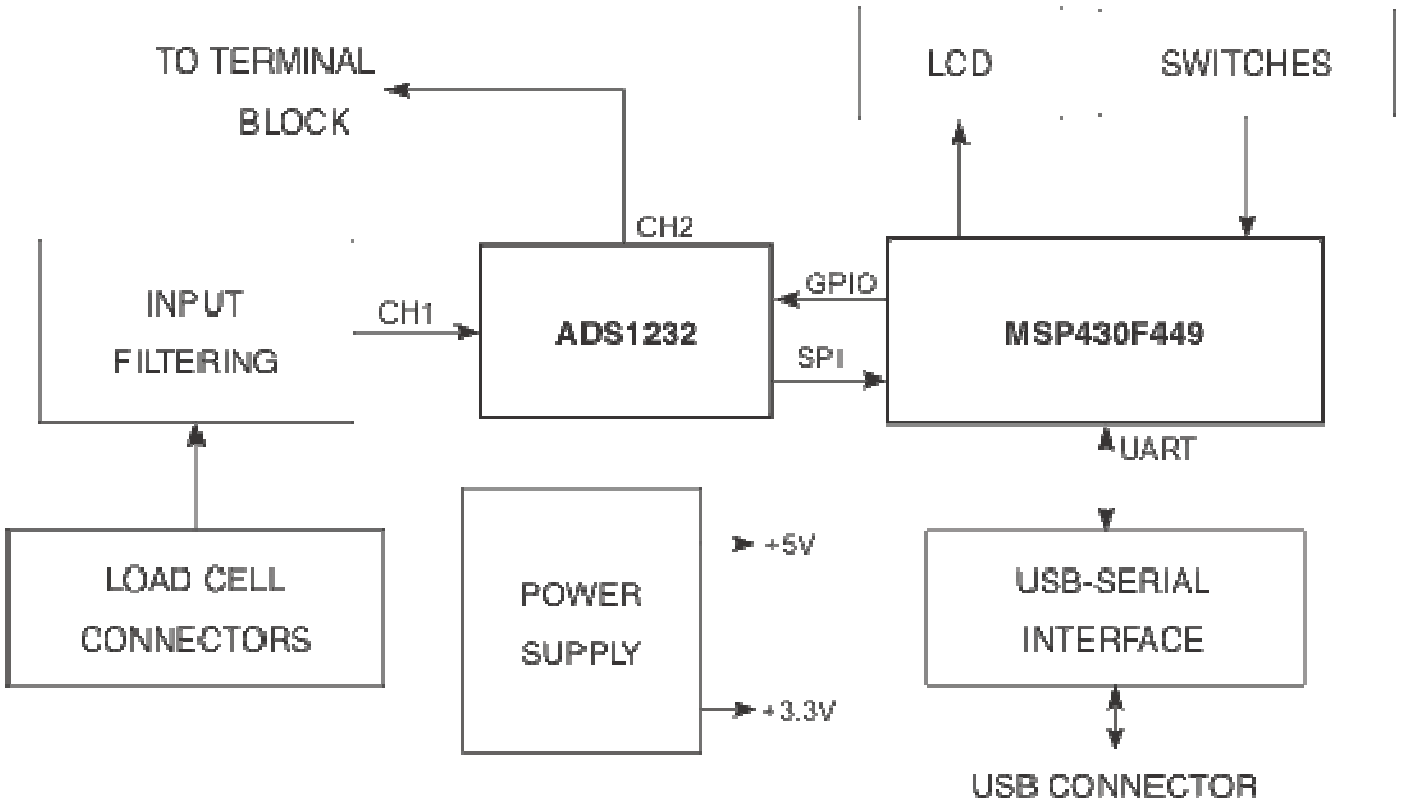
A plan to minimize analog circuit EMI susceptibility



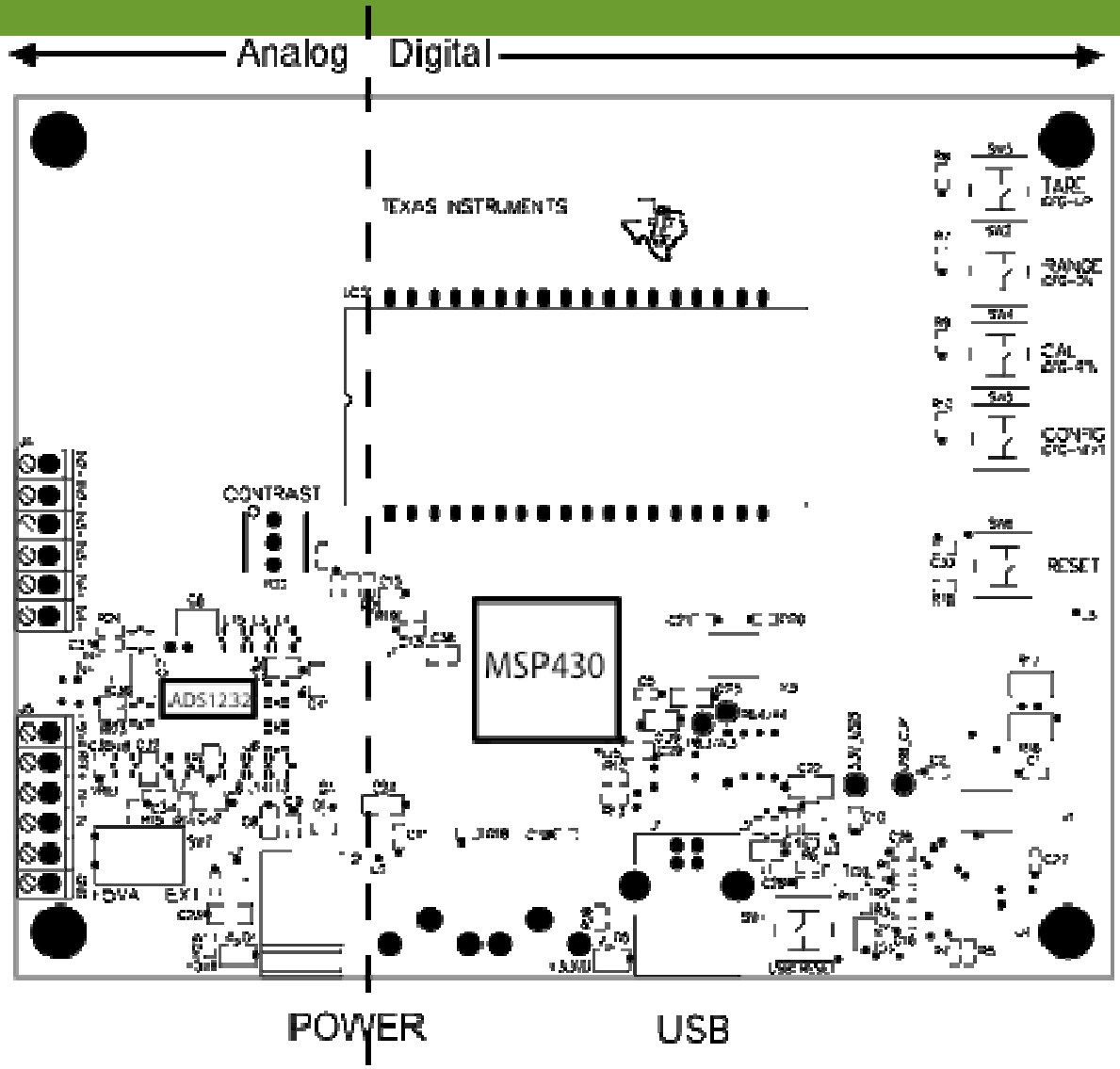
Enemy #3: Poor Grounds

- A good grounding scheme helps reduce the values of the “hidden” components.
- The key to good ground plane design is managing return currents
- Requires good floorplanning first.

Block Diagram

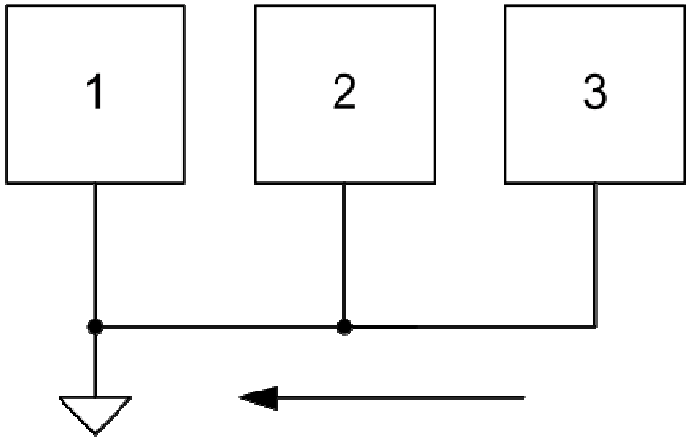


Component Placement



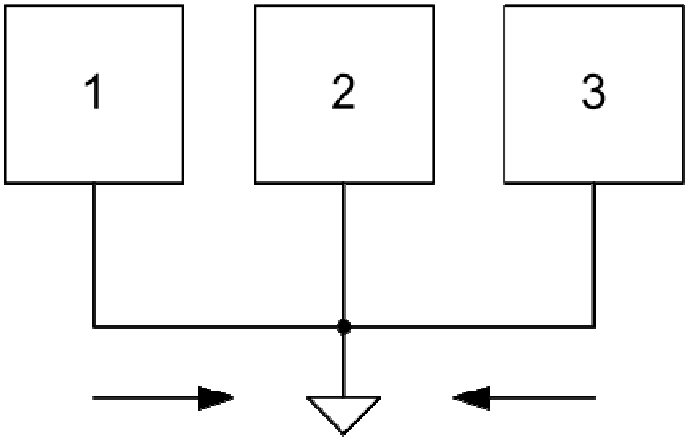
Single Point Grounding

Series



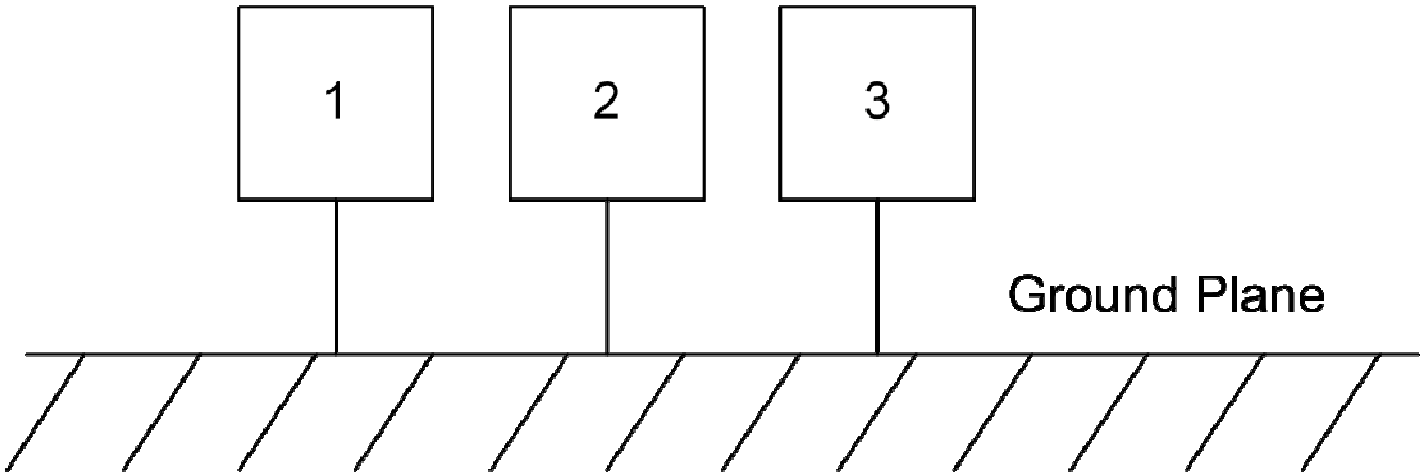
- Simple wiring
- Common impedance causes different potentials
- High impedance at high frequency (>10 kHz)

Parallel



- Complicated wiring
- Low differential potentials at low frequencies
- High impedance at high frequency (>10 kHz)

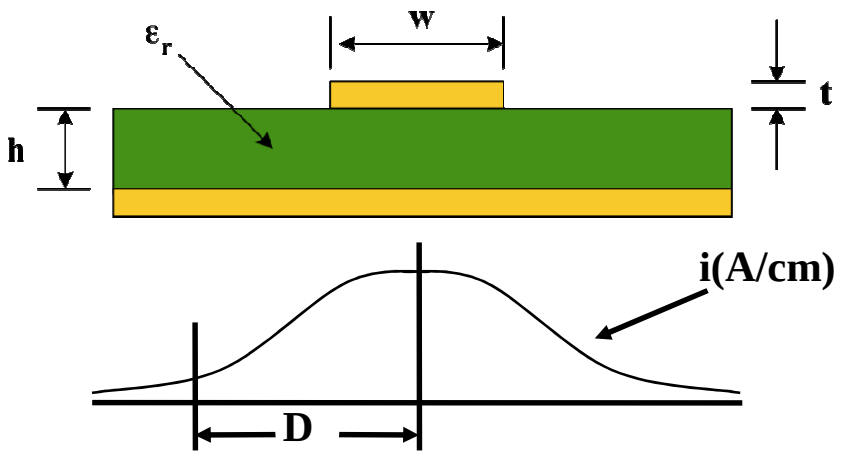
Multi Point Grounding



- Ground plane provides low impedance between circuits to minimize potential differences
- Also, reduces inductance of circuit traces
- Goal is to contain high frequency currents in individual circuits and keep out of ground plane

Current Density

$$i(A/cm) = \frac{I_O}{\pi\, h} \times \frac{1}{1 + \left(\frac{D}{h}\right)^2}$$



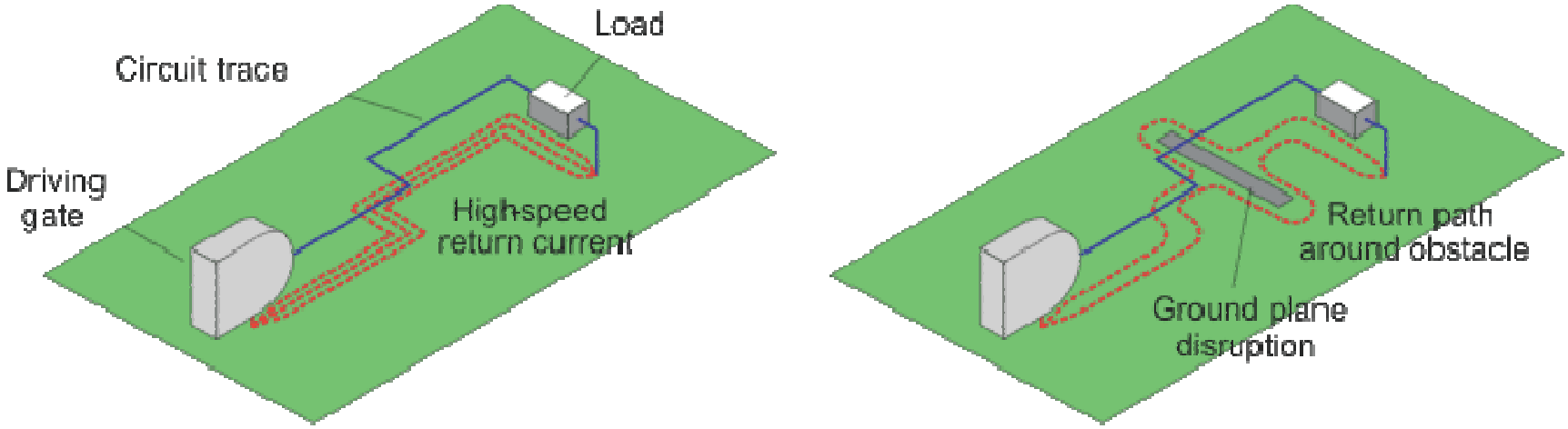
I_O = total signal current (A)

h = height of trace (cm)

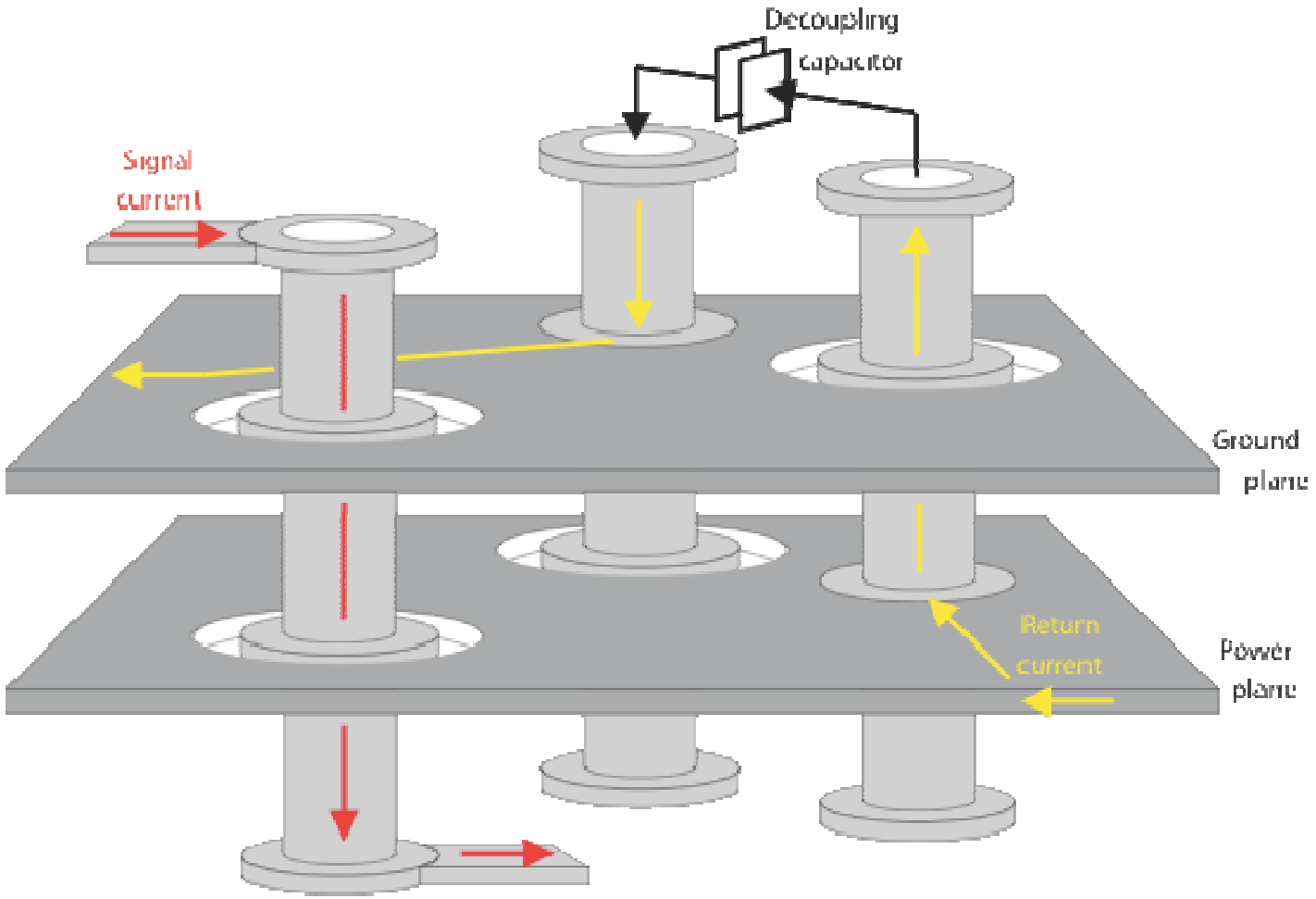
D = distance from trace (cm)

- Illustrates Return Current Flow is directly below the signal trace. This creates the path of least impedance.
- Must have Solid return path (i.e. Solid Ground Plane) under the signal trace to maintain homogeneous nature of current density.

Slots in Ground Plane

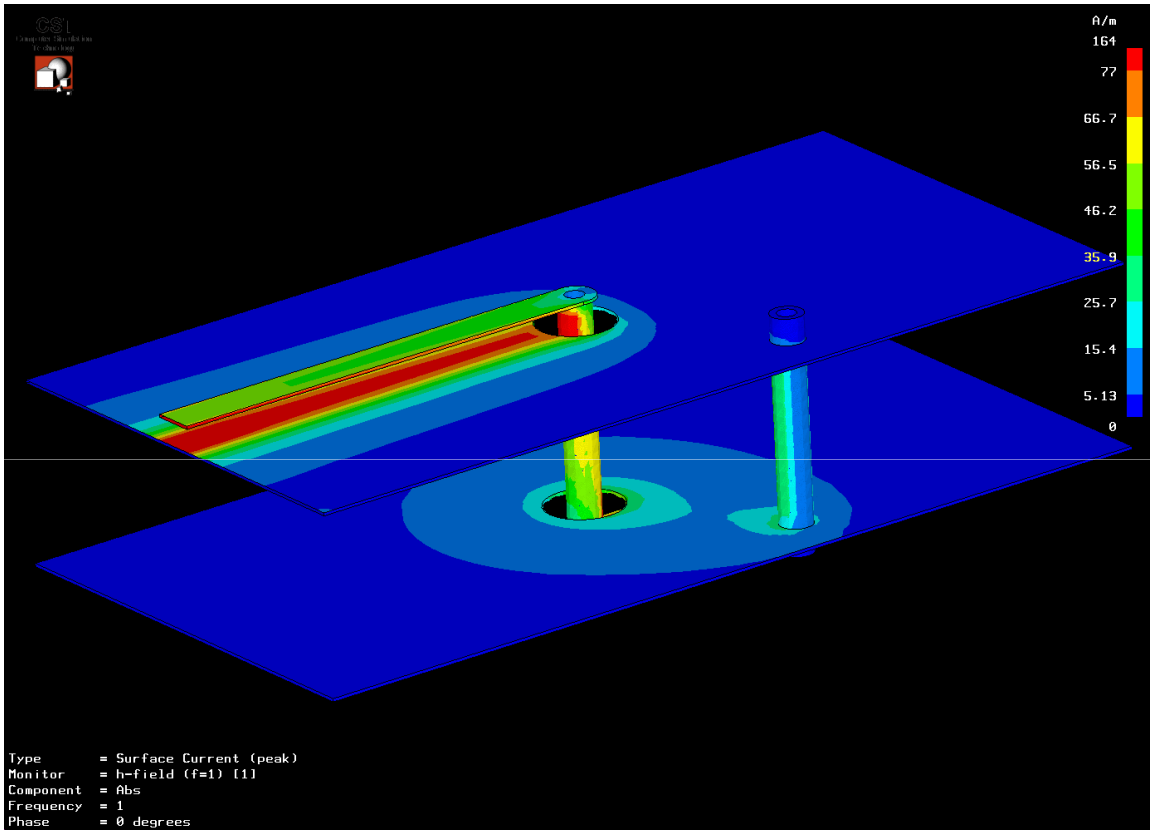


Return Current Paths



Taking a Look at Vias

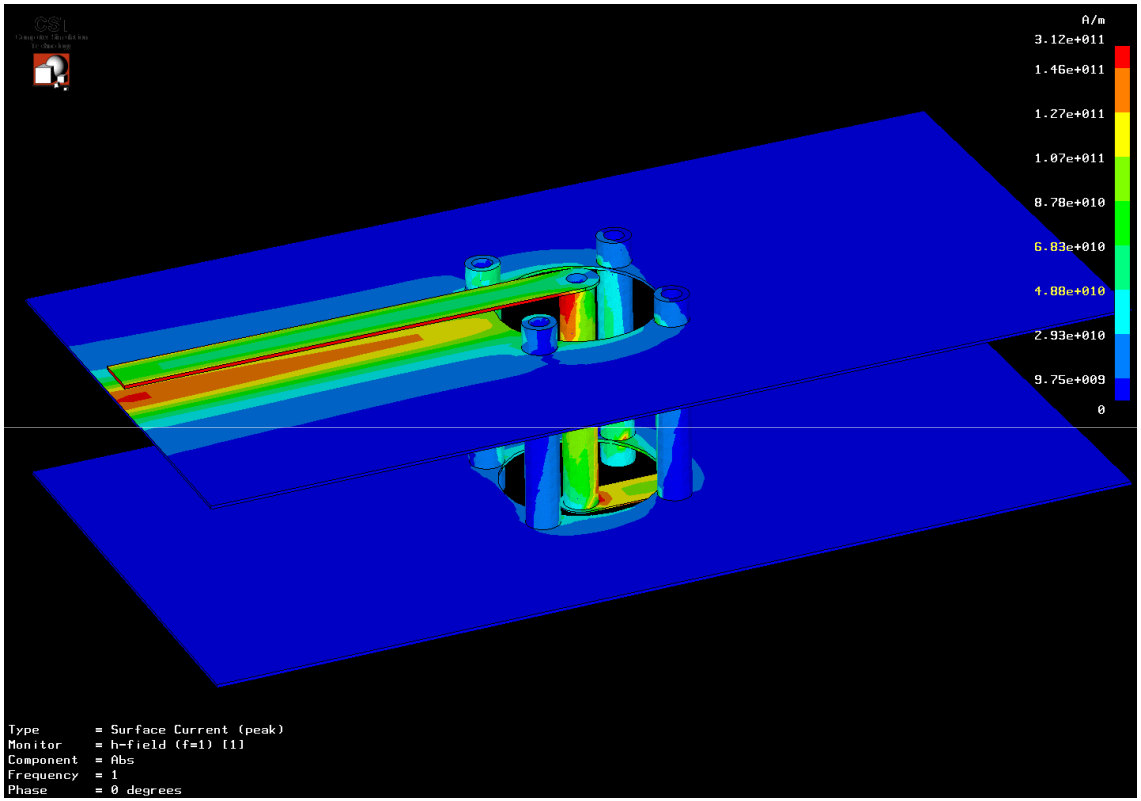
- Must have Return Path Vias next to Signal Path Vias.
- Notice Large Current Density Area flow in return path.
- Will have a change in impedance with this configuration.



2-Layer PCB showing Current Density of PCB trace and Single Return Path Via.

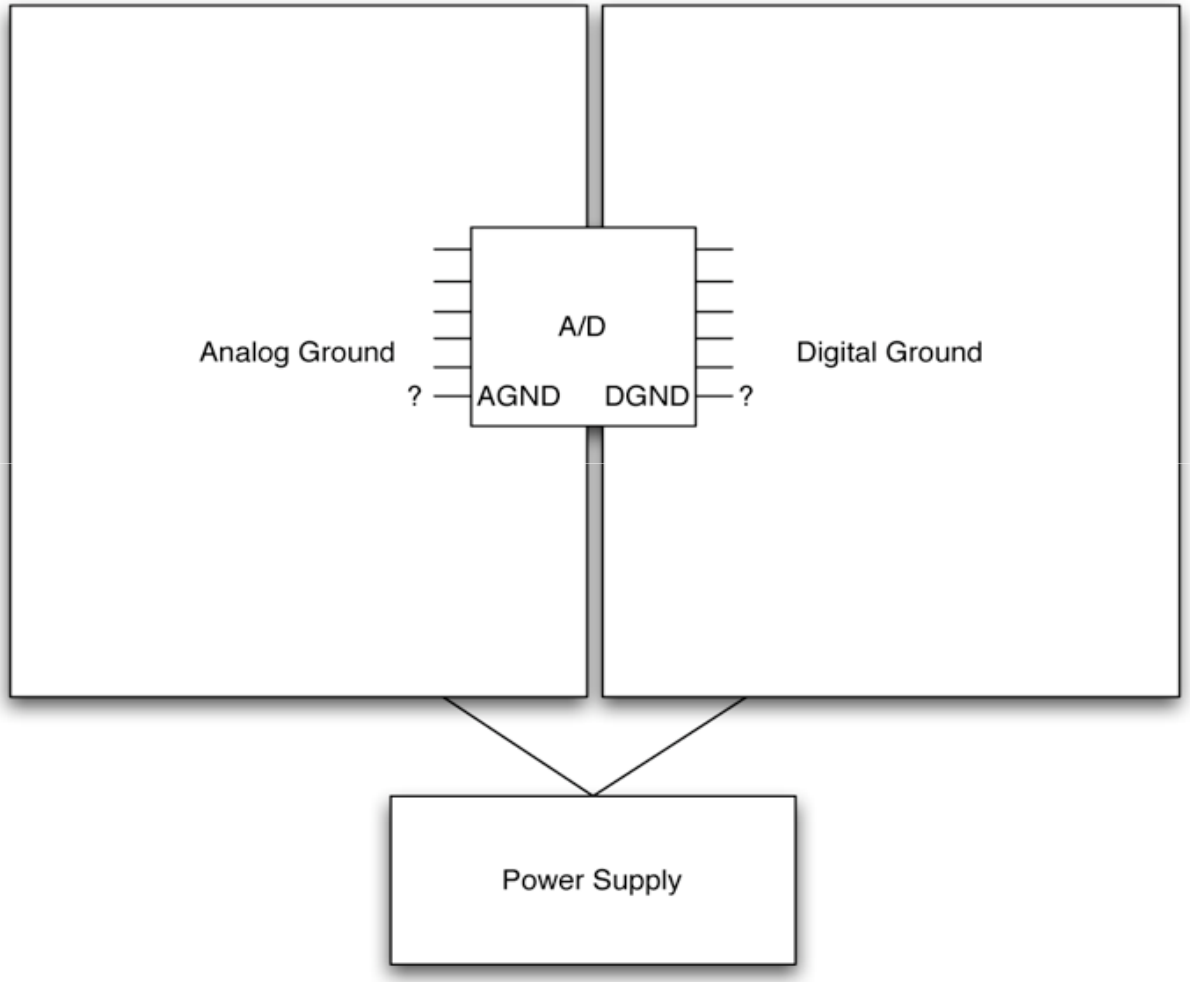
Controlled Impedance Vias

- Better Solution is to add Multiple Return Path Vias.
- Notice minimal Current Density Area Flow at vias.
- Improved impedance – reduces reflections.

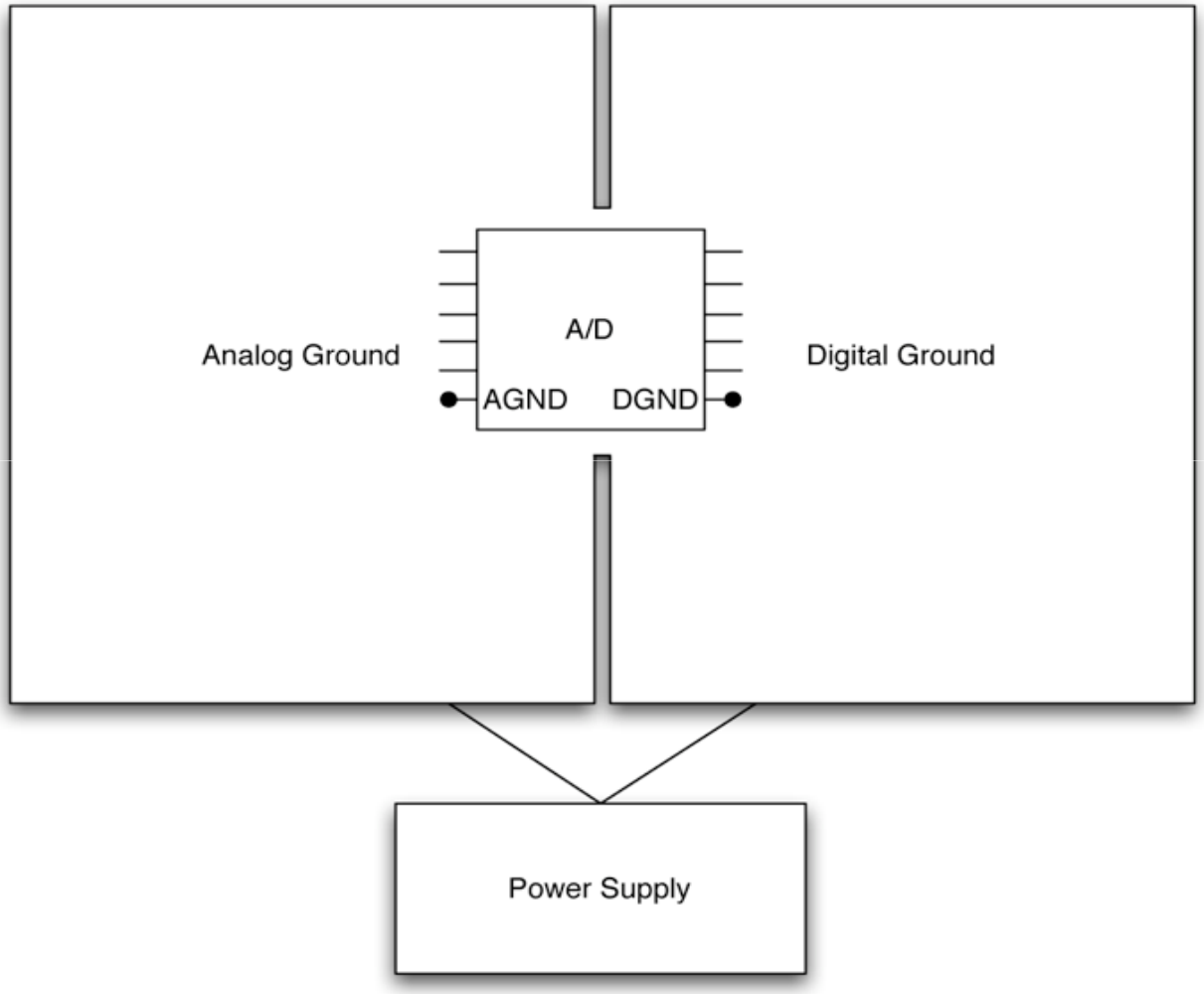


2-Layer PCB showing Current Density of PCB trace and Multiple Return Path Vias.

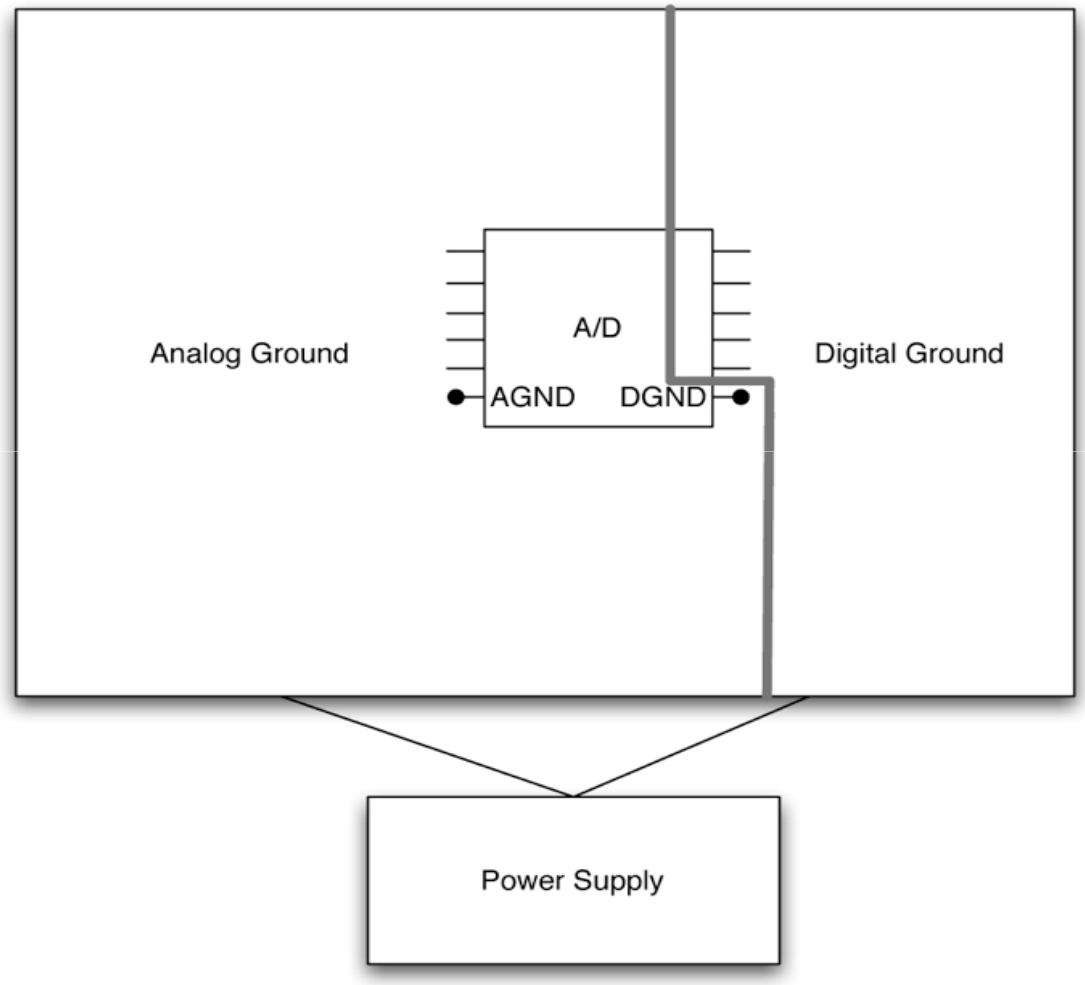
Split Grounds



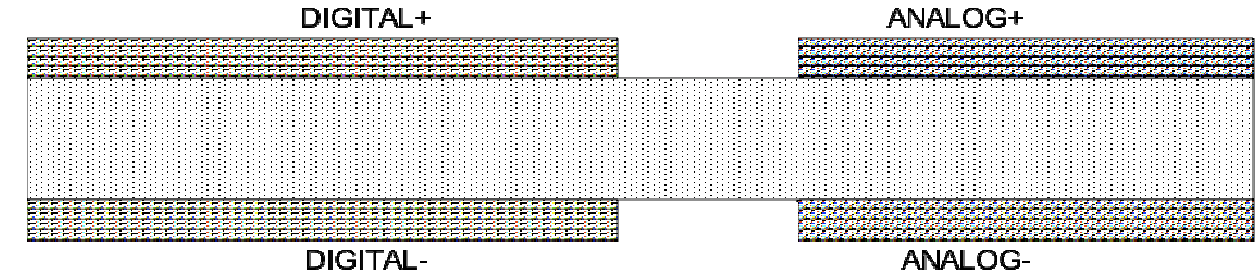
Split Ground Connected Under ADC

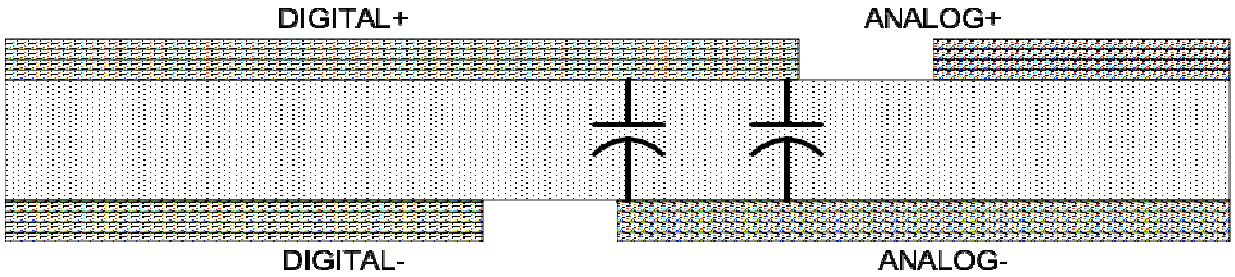


Connecting Both to Analog Ground

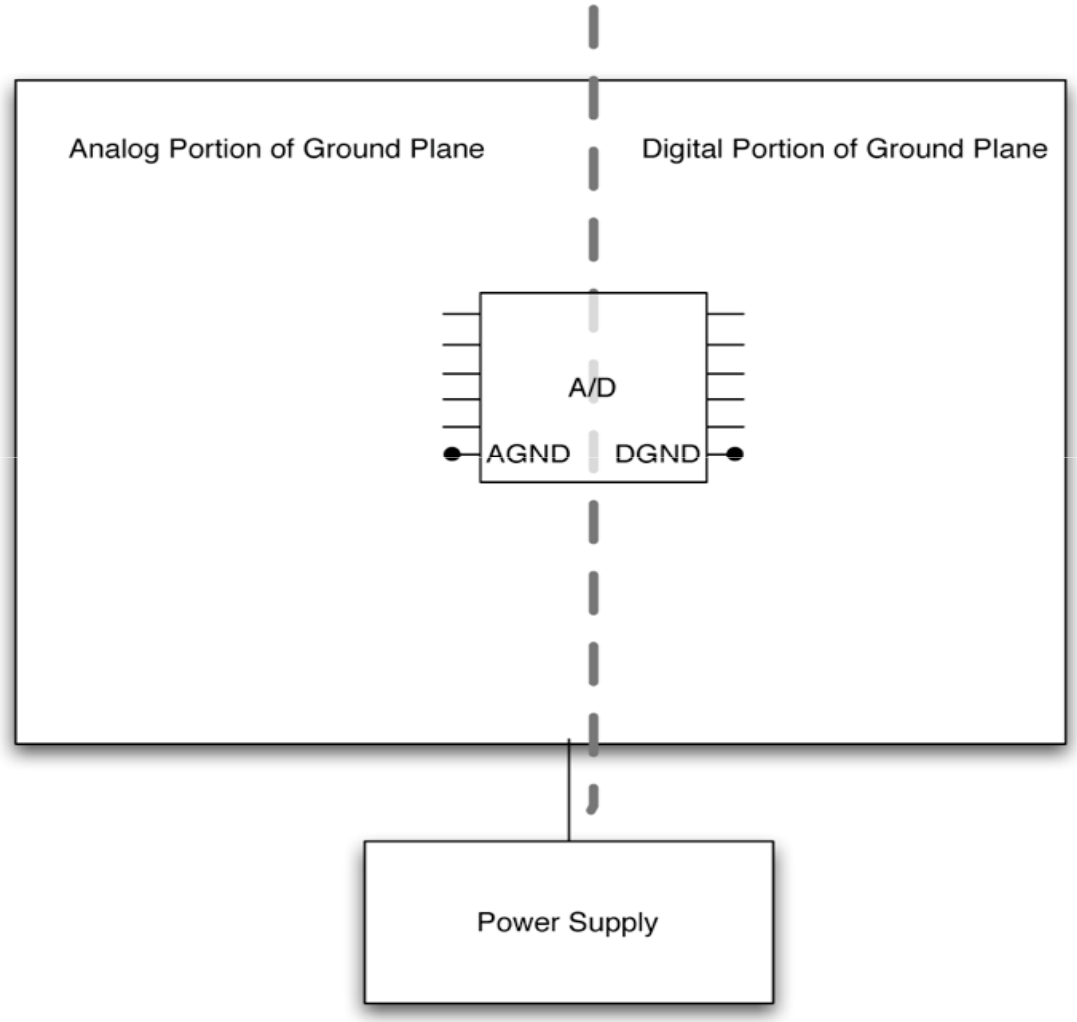


Ground Plane overlap

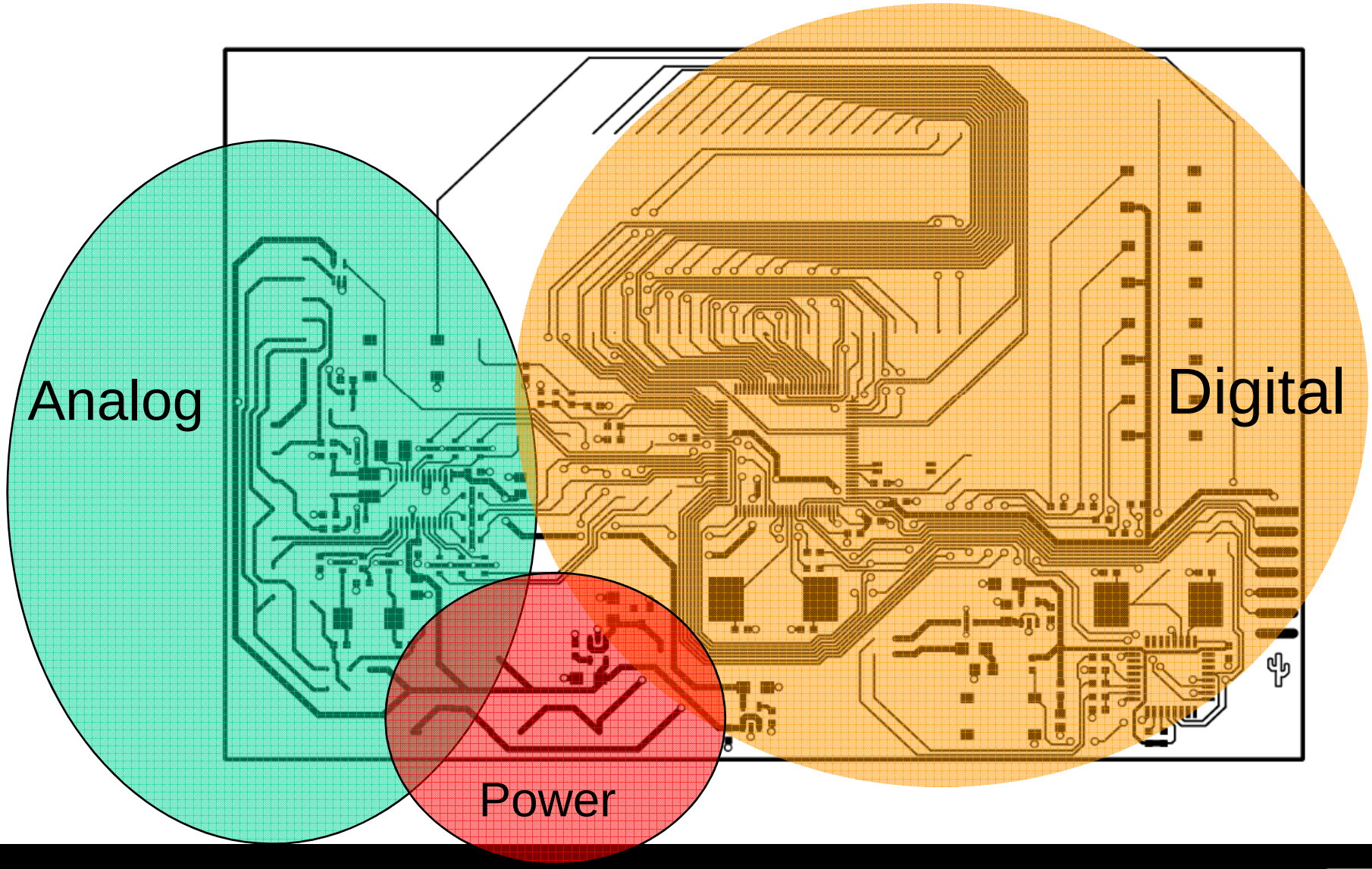




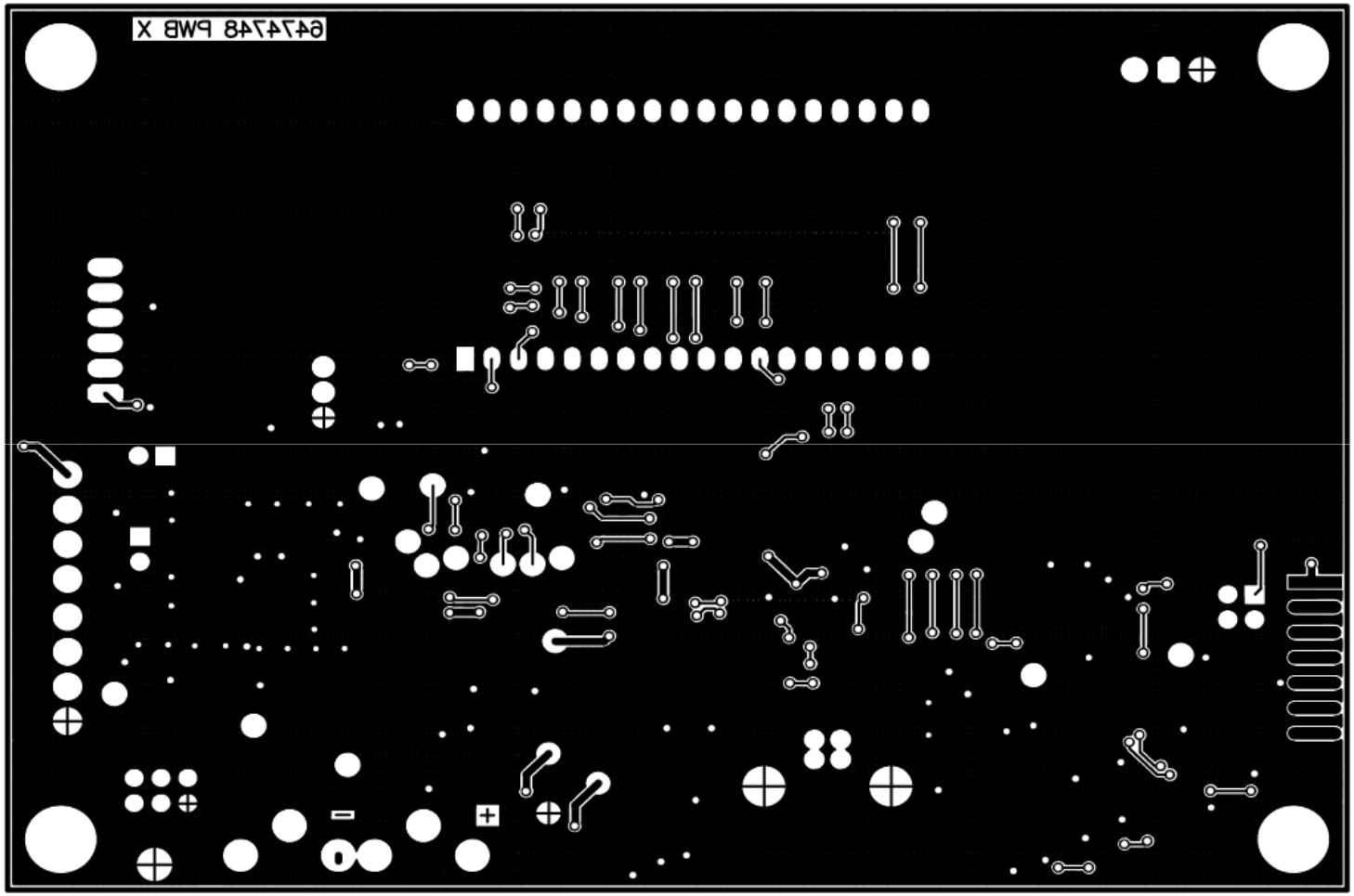
No Split


Analog Portion of Ground Plane
Digital Portion of Ground Plane
A/D
AGND
DGND
Power Supply

ADS1232REF Layout: Top



ADS1232REF Layout: Bottom



Thank You!
Any Questions?

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